



Intel® Arria® 10 FPGA Development Kit User Guide



Online Version



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1. Intel® Arria® 10 FPGA Development Kit Overview

The Intel® Arria® 10 GX FPGA development board provides a hardware platform for evaluating the performance and features of the Intel Arria 10 device.

1.1. General Description

Figure 1. Arria 10 GX Block Diagram

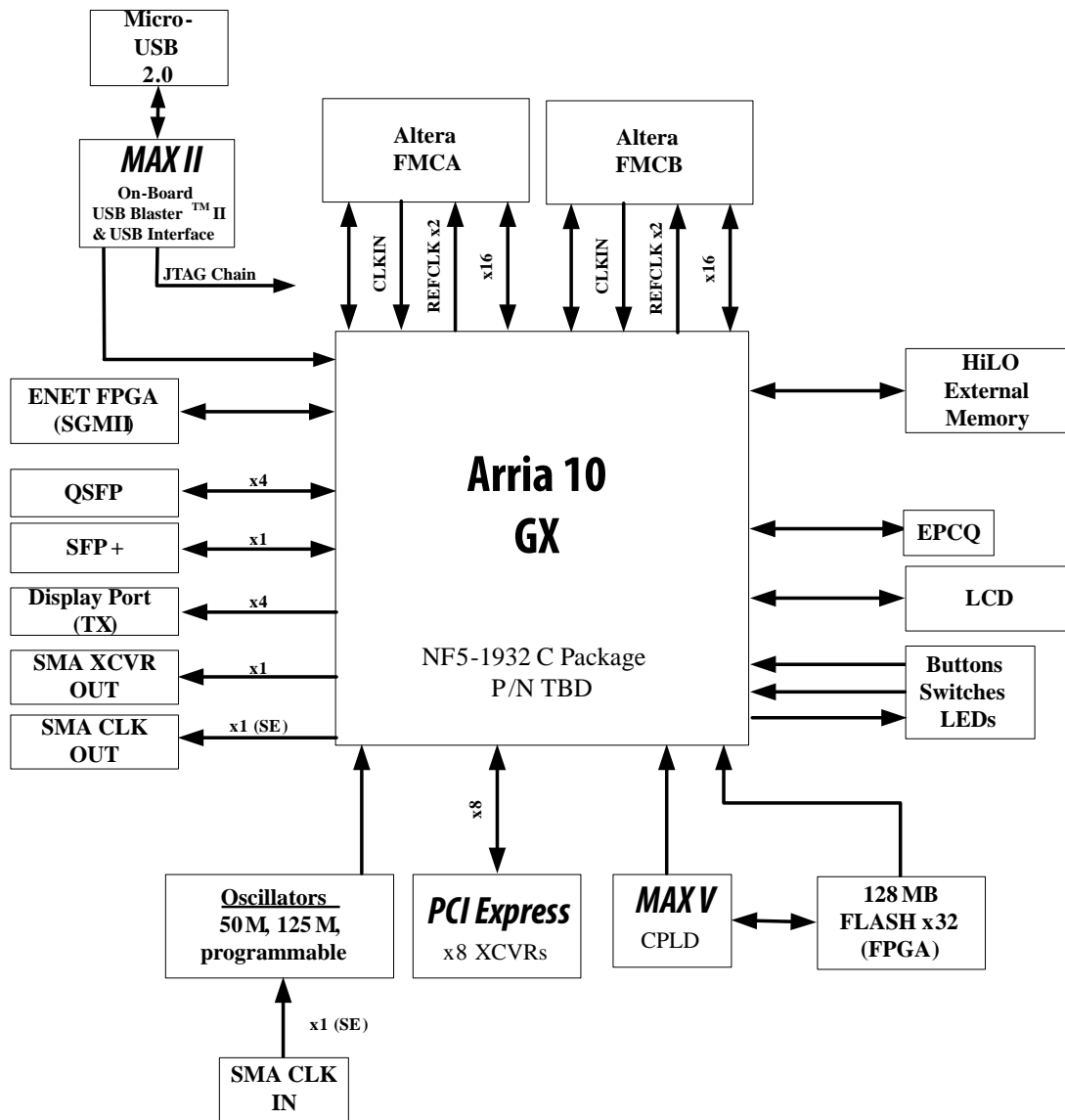


Figure 2. Overview of the Development Board Features (ES Edition)

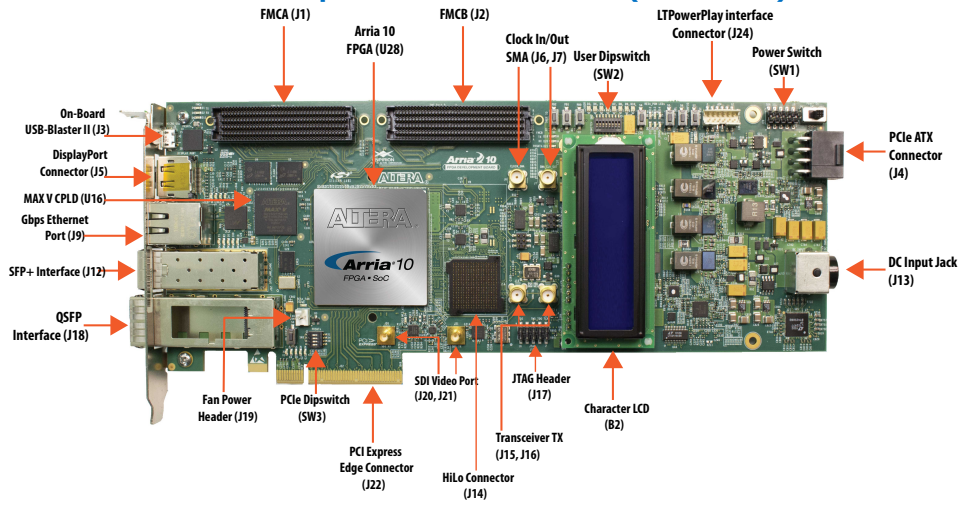
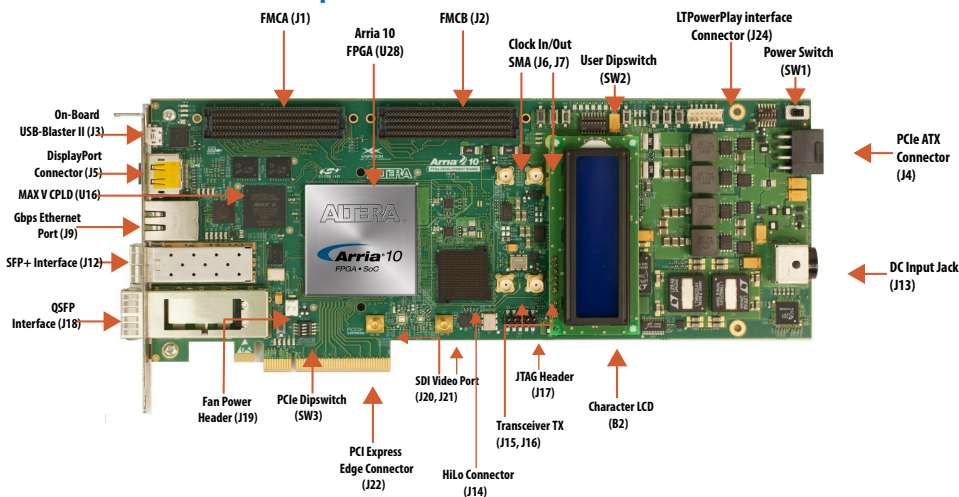


Figure 3. Overview of the Development Board Features



Related Information

[Board Components](#) on page 55
For details on the board components.

1.2. Recommended Operating Conditions

- Recommended ambient operating temperature range: 0C to 45C
- Maximum ICC load current: 80A
- Maximum ICC load transient percentage: 35%
- FPGA maximum power supported by the supplied heatsink/fan: 100W

1.3. Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a Vibration Environment.

2. Getting Started

2.1. Installing the Subscription Edition Software

The Quartus Prime Standard Edition software provides the necessary tools used for developing hardware and software for Altera devices.

Included in the Quartus Prime Standard Edition software are the Quartus Prime software, the Nios II[®] EDS, and the MegaCore IP Library. To install the Altera development tools, download the Quartus Prime Standard Edition software from the Quartus Prime Standard Edition software page of the Altera website.

Related Information

[Quartus Prime Software Page](#)

2.1.1. Activating Your License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus Prime software. After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus Prime software. To continue using the Quartus Prime software, you should download the free Quartus Prime Lite Edition or purchase a subscription to Quartus Prime Standard or Pro software.

Before using the Quartus Prime software, you must activate your license, identify specific users and computers, and obtain and install a license file. If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the [myAltera Account Sign In](#) web page, and click **Sign In**.
2. On the myAltera Home web page, click the Self-Service Licensing Center link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
4. On the Self-Service Licensing Center web page, click the Find it with your License Activation Code link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.
6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products**, and click **Close**.
8. When licensing is complete, Altera emails a `license.dat` file to you. Store the file on your computer and use the License Setup page of the **Options** dialog box in the Quartus Prime software to enable the software.

Related Information

- [Altera Software Installation and Licensing](#)
Comprehensive information for installing and licensing Altera software.
- [myAltera Account Sign In web page](#)

2.2. Development Kit Package

1. Download the Arria 10 FPGA Development Kit package zip file available at the Intel website.
2. Extract the contents of the zip file to your hard drive.
The development kit directory structure is shown in the following figure.

Figure 4. Installed Development Kit Directory Structure

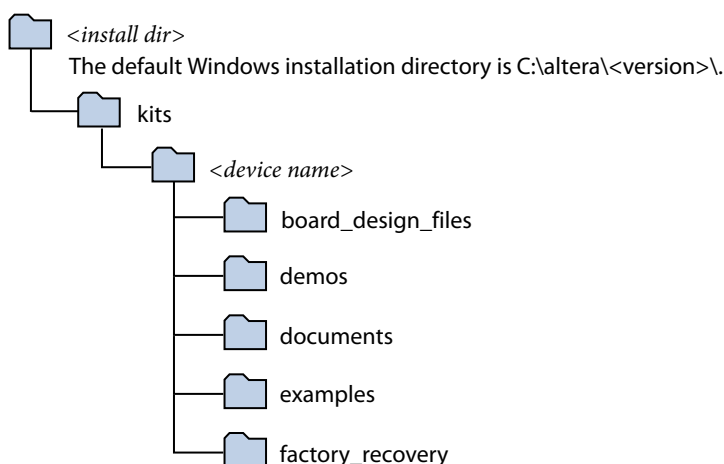


Table 1. Installed Directory Contents

| Directory Name | Description of Contents |
|--------------------|--|
| board_design_files | Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design. |
| demos | Contains demonstration applications when available. |
| documents | Contains the documentation. |
| examples | Contains the sample design files for this kit. |
| factory_recovery | Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents. |

Related Information

[Link to download zip file for the Arria 10 Development Kit Package](#)

2.3. Installing the USB-Blaster Driver

The development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board USB-Blaster II driver on the host computer.

Installation instructions for the On-Board USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

Related Information

[Altera Programming Cable Driver Information](#)

Click on the link for your operating system.

3. Development Board Setup

This section describes how to apply power to the board and provides default switch and jumper settings.

3.1. Applying Power to the Board

This development kit ships with its board switches preconfigured to support the design examples in the kit.

If you suspect that your board might not be currently configured with the default settings, follow the instructions in the Default Switch and Jumper Settings section of this chapter.

1. The development board ships with design examples stored in the flash memory device. To load the design stored in the factory portion of flash memory, verify SW6.4 is set to ON. This is the default setting.
2. Connect the supplied power supply to an outlet and the DC Power Jack (J13) on the FPGA board.

Caution: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

3. Set the power switch (SW1) to the on position.

When the board powers up, the parallel flash loader (PFL) on the MAX V reads a design from flash memory and configures the FPGA. When the configuration is complete, green LEDs illuminate signaling the device configured successfully. If the configuration fails, the red LED illuminates.

3.2. Default Switch and Jumper Settings

This topic shows you how to restore the default factory settings and explains their functions.

Caution: Do not install or remove jumpers (shunts) while the development board is powered on.

Figure 5. Default Switch and Jumper Settings on the Top

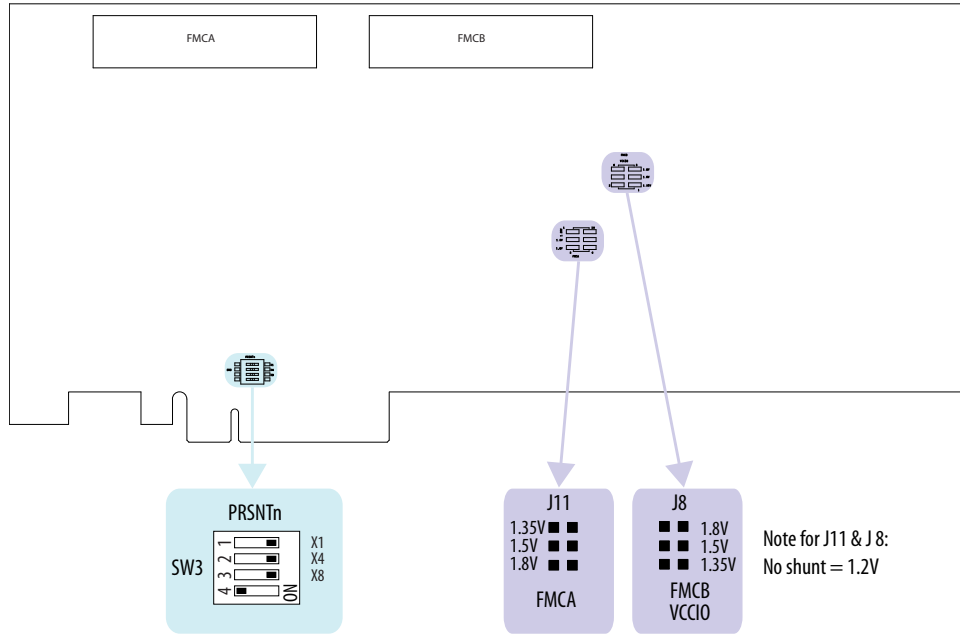
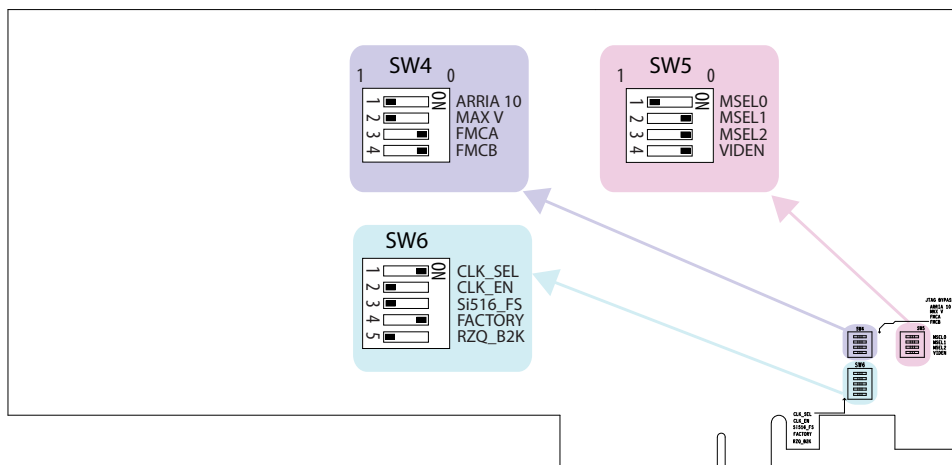


Figure 6. Default Switch Settings on the Bottom



1. Set DIP switch bank (SW3) to match the following table.

Table 2. SW3 DIP PCIe Switch Default Settings (Board Top)

| Switch | Board Label | Function | Default Position |
|--------|-------------|-----------------------------------|------------------|
| 1 | x1 | ON for PCIe x1 | ON |
| 2 | x4 | ON for PCIe x4 | ON |
| 3 | x8 | ON for PCIe x8 | ON |
| 4 | — | OFF for 1.35 V MEM_VDD power rail | OFF |

- If all of the jumper blocks are open, the FMCA and FMCB VCCIO value is 1.2 V. To change that value, add shunts as shown in the following table.

Table 3. Default Jumper Settings for the FPGA Mezzanine Card (FMC) Ports (Board Top)

| Board Reference | Board Label | Description |
|-----------------|-------------|--------------------------------------|
| J8 pins 1-2 | 1.35V | 1.35 V FMCB V _{CCIO} select |
| J8 pins 3-4 | 1.5V | 1.5 V FMCB V _{CCIO} select |
| J8 pins 5-6 | 1.8V | 1.8 V FMCB V _{CCIO} select |
| J11 pins 1-2 | 1.35V | 1.35 V FMCA V _{CCIO} select |
| J11 pins 3-4 | 1.5V | 1.5 V FMCA V _{CCIO} select |
| J11 pins 5-6 | 1.8V | 1.8 V FMCA V _{CCIO} select |

- Set DIP switch bank (SW4) to match the following table.

Table 4. SW4 JTAG DIP Switch Default Settings (Board Bottom)

| Switch | Board Label | Function | Default Position |
|--------|-------------|---|------------------|
| 1 | ARRIA 10 | OFF to enable the Arria 10 in the JTAG chain | OFF |
| 2 | MAX V | OFF to enable the MAX V in the JTAG chain | OFF |
| 3 | FMCA | ON to bypass the FMCA connector in the JTAG chain | ON |
| 4 | FMCB | ON to bypass the FMCB connector in the JTAG chain | ON |

- Set DIP switch bank (SW5) to match the following table.

Table 5. SW5 DIP Switch Default Settings (Board Bottom)

| Switch | Board Label | Function | Default Position |
|--------|-------------|---|------------------|
| 1 | MSEL0 | OFF for MSEL0 = 1; for FPP standard mode | OFF |
| 2 | MSEL1 | ON for MSEL1 = 0; for FPP standard mode | ON |
| 3 | MSEL2 | ON for MSEL2 = 0; for FPP standard mode | ON |
| 4 | VIDEN | OFF for enabling VID_EN for the Smart Voltage ID (SmartVID) feature | ON |

- Set DIP switch bank (SW6) to match the following table.

Table 6. SW6 DIP Switch Default Settings (Board Bottom)

| Switch | Board Label | Function | Default Position |
|--------|-------------|--|------------------|
| 1 | CLK_SEL | ON for 100 MHz on-board clock oscillator selection OFF for SMA input clock selection | ON |
| 2 | CLK_EN | OFF for setting CLK_ENABLE signal high to the MAV V | OFF |
| 3 | Si516_FS | ON for setting the SDI REFCLK frequency to 148.35 MHz OFF for setting the SDI REFCLK frequency to 148.5 MHz | OFF |
| 4 | FACTORY | ON to load factory image from flash OFF to load user image #1 from flash | ON |
| 5 | RZQ_B2K | ON for setting RZQ resistor of Bank 2K to 99.17 ohm OFF for setting RZQ resistor of Bank 2K to 240 ohm | OFF |

3.3. Default Switch and Resistor Settings

This topic shows you how to restore the default factory settings and explains their functions.

Figure 7. Default Switch and Resistor Settings on the Top

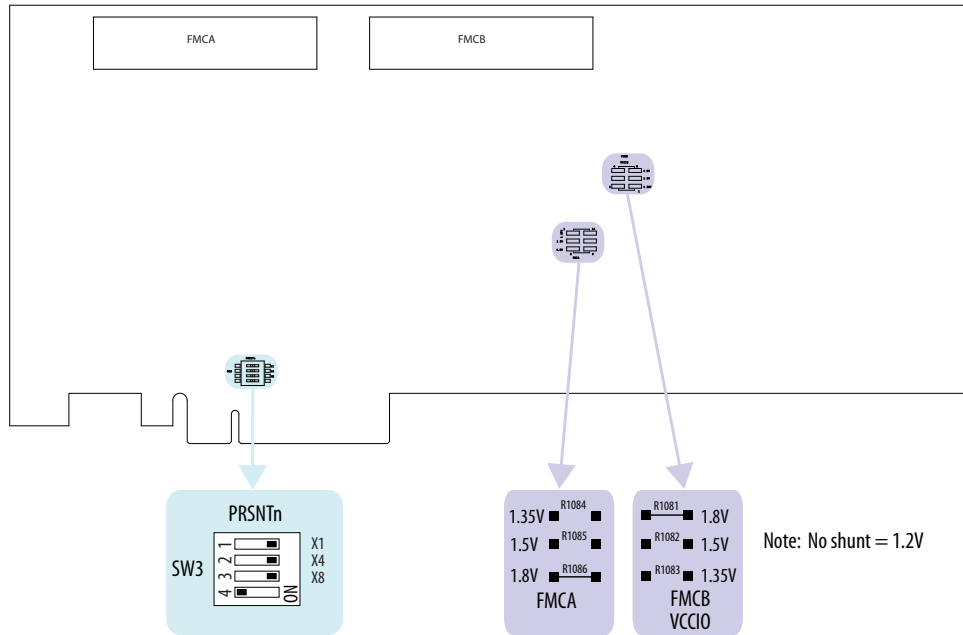
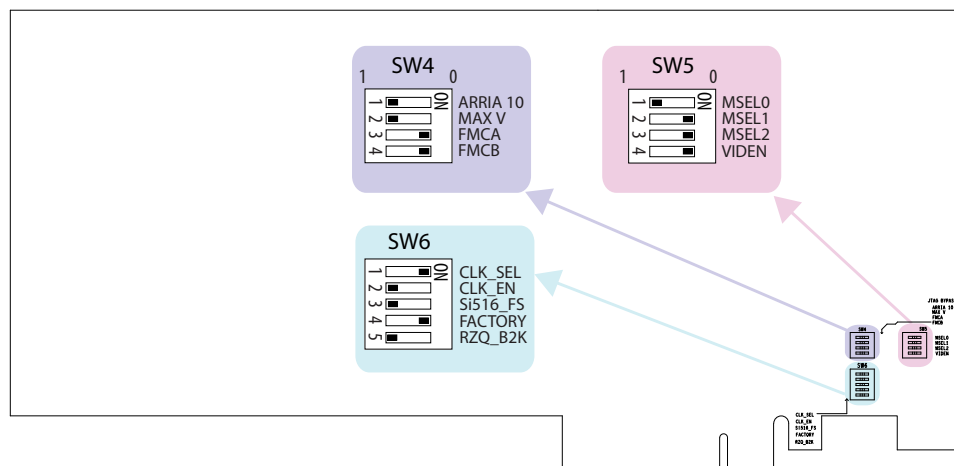


Figure 8. Default Switch Settings on the Bottom



1. Set DIP switch bank (SW3) to match the following table.

Table 7. SW3 DIP PCIe Switch Default Settings (Board Top)

| Switch | Board Label | Function | Default Position |
|--------|-------------|-----------------------------------|------------------|
| 1 | x1 | ON for PCIe x1 | ON |
| 2 | x4 | ON for PCIe x4 | ON |
| 3 | x8 | ON for PCIe x8 | ON |
| 4 | — | OFF for 1.35 V MEM_VDD power rail | OFF |

- If all of the resistors are open, the FMCA and FMCB VCCIO value is 1.2 V. To change that value, add resistors as shown in the following table.

Table 8. Default Resistor Settings for the FPGA Mezzanine Card (FMC) Ports (Board Top)

| Board Reference | Board Label | Description |
|-----------------|-------------|---|
| R1083 | 1.35V | 1.35 V FMCB V _{CCIO} select |
| R1082 | 1.5V | 1.5 V FMCB V _{CCIO} select |
| R1081 | 1.8V | 1.8 V FMCB V _{CCIO} select <i>Note: A 0 Ohm resistor is installed by default.</i> |
| R1084 | 1.35V | 1.35 V FMCA V _{CCIO} select |
| R1085 | 1.5V | 1.5 V FMCA V _{CCIO} select |
| R1086 | 1.8V | 1.8 V FMCA V _{CCIO} select <i>Note: A 0 Ohm resistor is installed by default.</i> |

- Set DIP switch bank (SW4) to match the following table.

Table 9. SW4 JTAG DIP Switch Default Settings (Board Bottom)

| Switch | Board Label | Function | Default Position |
|--------|-------------|---|------------------|
| 1 | ARRIA 10 | OFF to enable the Arria 10 in the JTAG chain | OFF |
| 2 | MAX V | OFF to enable the MAX V in the JTAG chain | OFF |
| 3 | FMCA | ON to bypass the FMCA connector in the JTAG chain | ON |
| 4 | FMCB | ON to bypass the FMCB connector in the JTAG chain | ON |

- Set DIP switch bank (SW5) to match the following table.

Table 10. SW5 DIP Switch Default Settings (Board Bottom)

| Switch | Board Label | Function | Default Position |
|--------|-------------|---|------------------|
| 1 | MSEL0 | OFF for MSEL0 = 1; for FPP standard mode | OFF |
| 2 | MSEL1 | ON for MSEL1 = 0; for FPP standard mode | ON |
| 3 | MSEL2 | ON for MSEL2 = 0; for FPP standard mode | ON |
| 4 | VIDEN | OFF for enabling VID_EN for the Smart Voltage ID (SmartVID) feature | ON |

- Set DIP switch bank (SW6) to match the following table.

Table 11. SW6 DIP Switch Default Settings (Board Bottom)

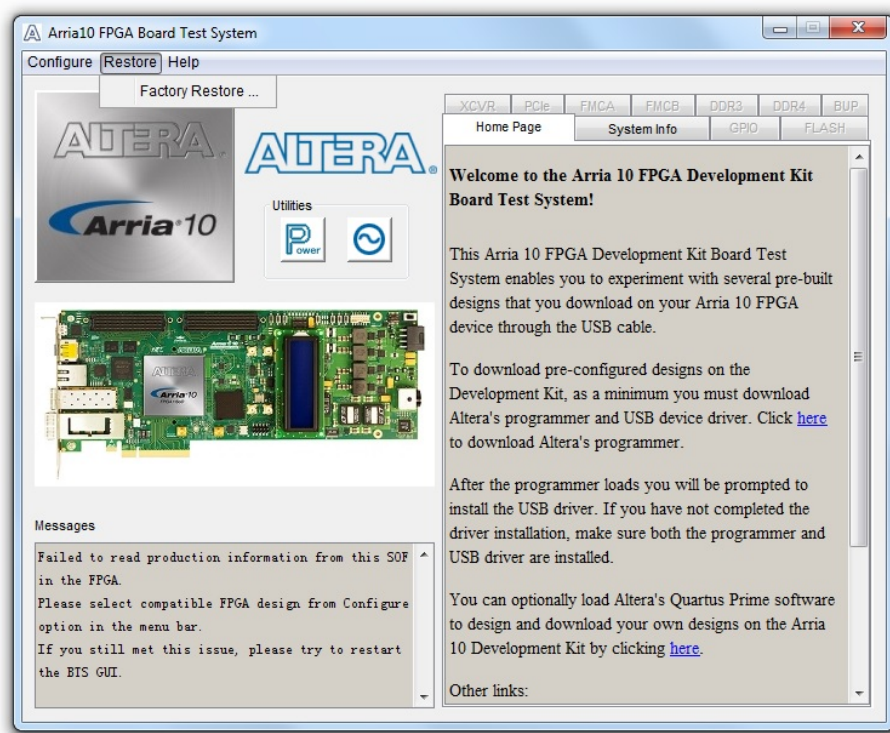
| Switch | Board Label | Function | Default Position |
|--------|-------------|--|------------------|
| 1 | CLK_SEL | ON for 100 MHz on-board clock oscillator selection OFF for SMA input clock selection | ON |
| 2 | CLK_EN | OFF for setting CLK_ENABLE signal high to the MAV V | OFF |
| 3 | Si516_FS | ON for setting the SDI REFCLK frequency to 148.35 MHz OFF for setting the SDI REFCLK frequency to 148.5 MHz | OFF |
| 4 | FACTORY | ON to load factory image from flash OFF to load user image #1 from flash | ON |
| 5 | RZQ_B2K | ON for setting RZQ resistor of Bank 2K to 99.17 ohm OFF for setting RZQ resistor of Bank 2K to 240 ohm | OFF |

3.4. Factory Reset

To do a factory reset, follow these steps:

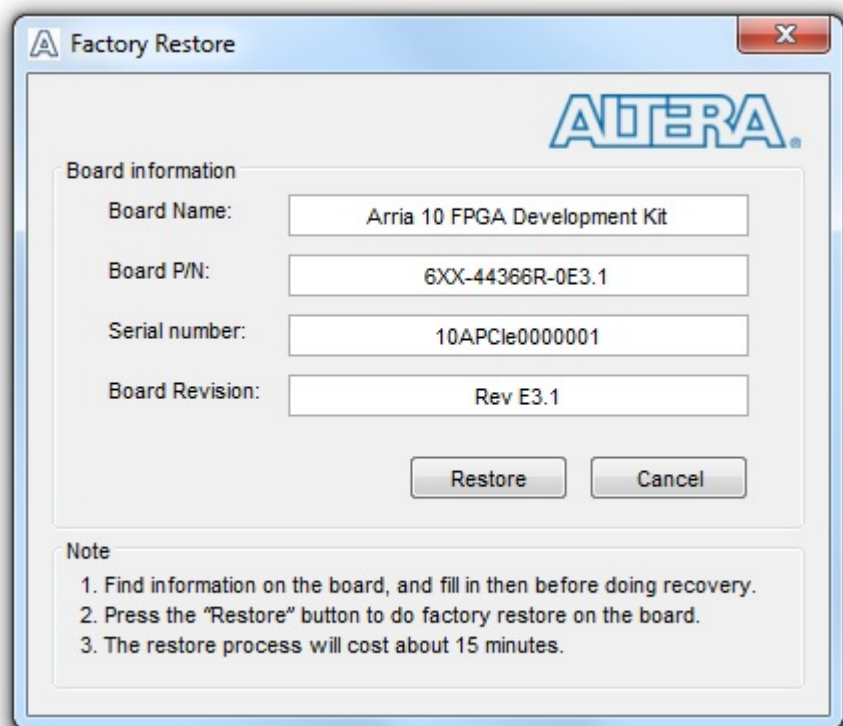
1. Install the latest Altera software tools, including the Quartus Prime software, Nios II processor, and IP functions. If necessary, download the Quartus Prime Pro Edition software from the [Altera Download Center](#).
2. Set the board switches to the factory default settings described in "[Default Switch and Resistor Settings](#)".
3. Open the GUI application "**BoardTestSystem.exe**".
 - a. Launch the Nios II command shell, change to directory to <package dir>\examples\board_test_system\, and then type in **./BoardTestSystem.exe** to open the GUI.
 - b. Change directory to <package dir>\examples\board_test_system\, and then double click "**BoardTestSystem.exe**" to open the GUI.
4. Select "**Restore -> Factory Restore**".

Figure 9. Arria 10 FPGA Board Test System Factory Restore Select



5. Set the correct board information and then click restore. The restore process takes about 10 minutes.

Figure 10. Factory Restore Window



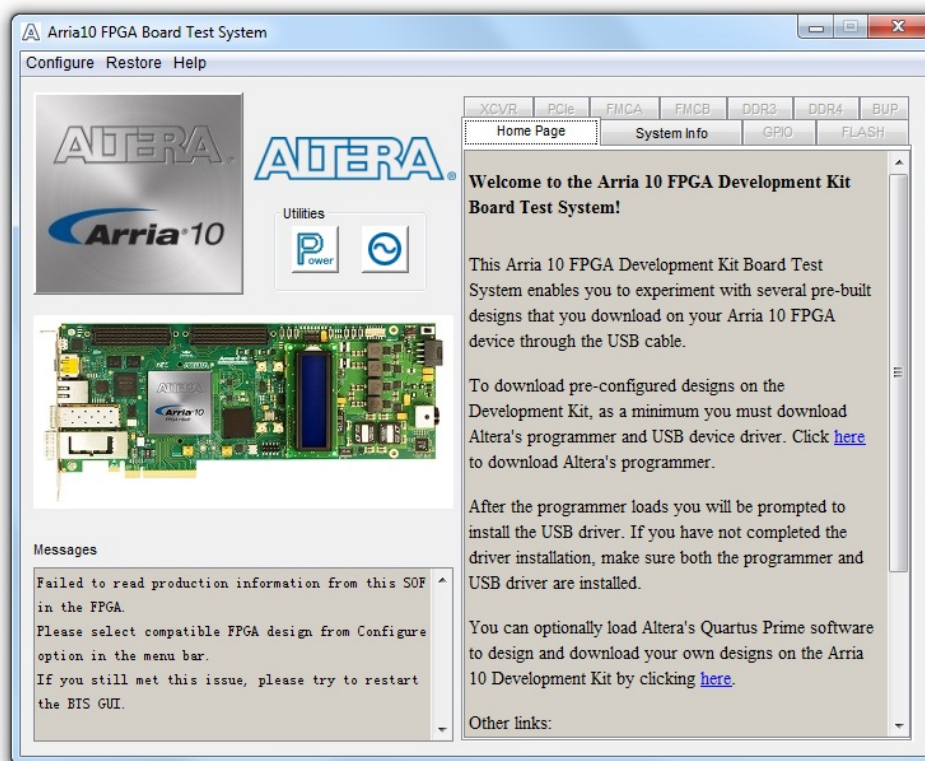
Related Information

- [Board Update Portal](#) on page 52
- [Using the Board Update Portal to Update User Designs](#) on page 54

4. Board Test System

The Board Test System (BTS) provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

Figure 11. Board Test System GUI



While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing. Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The BTS communicates over the JTAG bus to a test design running in the FPGA. The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap[®] II Embedded Logic Analyzer. Because the BTS is designed based on the Quartus Programmer and System Console, be sure to close other applications before you use the BTS application.

4.1. Preparing the Board

With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ-45 connector.
3. Check the development board switches and jumpers are set according to your preferences. See the “Factory Default Switch and Jumper Settings” section.
4. Set the load selector switch (SW6.4) to OFF for user hardware1 (page #1).

The development board ships with the CFI flash device preprogrammed with a default:

- Factory FPGA configuration for running the Board Update Portal design example
 - User configuration for running the Board Test System demonstration
5. Turn on the power to the board. The board loads the design stored in the user hardware1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO, Ethernet, and flash memory tests.

To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Related Information

[Default Switch and Jumper Settings](#) on page 12

4.2. Running the Board Test System

To run the Board Test System (BTS), navigate to the `<package_dir>\examples\board_test_system` directory and run the `BoardTestSystem.exe` application.

On Windows, you can also run the BTS from the **Start ► All Programs ► Altera** menu.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The development board's flash memory ships preconfigured with the design that corresponds to the GPIO tab.

Note: The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software. It sets the environment variable `$QUARTUS_ROOTDIR` automatically. The Board Test System uses this environment variable to locate the Quartus Prime library.

The BTS will pick up the Quartus Programmer to configure the FPGA device on your development kit. Make sure the Quartus Prime software you are using is the version supporting the FPGA silicon on the board.

4.3. Version Selector

The BTS will prompt you with a Version Selector window once opened. You can also open the Version Selector window through the **Configure** tab by clicking **Select Silicon Version**. Select the silicon version of the Arria 10 device that is installed on your board.

Figure 12. Configure Tab Version Selector Option

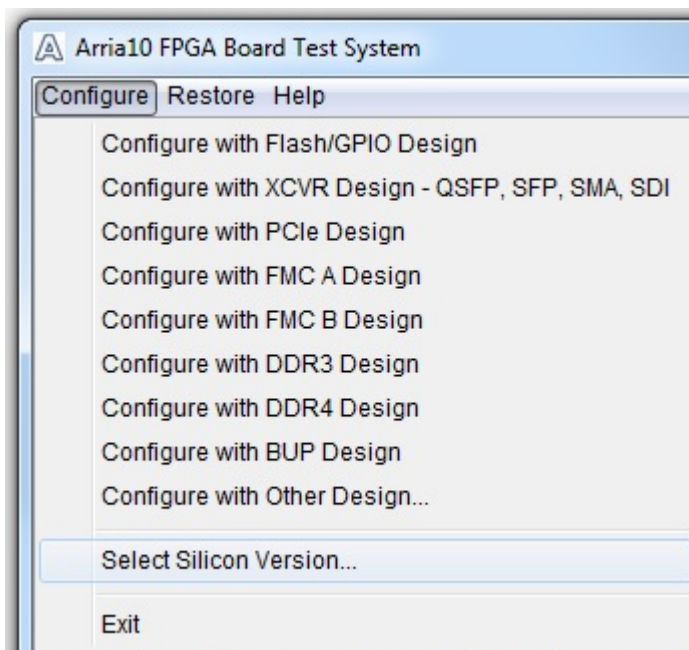


Figure 13. Version Selector



If you do not know, or are unsure of the version, enter the board serial number in the box on the right and the software will pick the right version based on the table below. The numbers here are the last 3-4 digits of the serial number which can be found on the bottom of your board.

Figure 14. Board Serial Number Sticker



Table 12. Serial Number to Arria 10 Silicon Revision

| Serial Number | Arria 10 Silicon Revision |
|-------------------------|---------------------------|
| 10APCIe000[< 0332] | ES2 |
| 10APCIe000[0332 - 0383] | PRD-1 |
| 10APCIe000[0500 - 0999] | ES3 |
| 10APCIe000[1000+] | PRD |

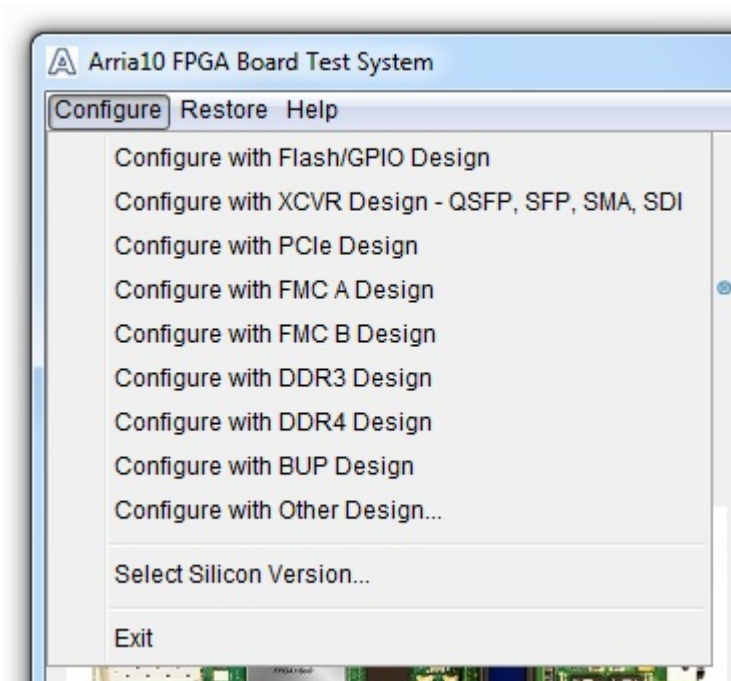
4.4. Using the Board Test System

This section describes each control in the Board Test System application.

4.4.1. Using the Configure Menu

Use the Configure menu to select the design you want to use. Each design example tests different board features. Choose a design from this menu and the corresponding tabs become active for testing.

Figure 15. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. On the **Configure** menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design to the FPGA.
3. When configuration finishes, close the Quartus Programmer if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

If you use the Quartus Programmer for configuration, rather than the Board Test System GUI, you may need to restart the GUI.

4.4.2. The System Info Tab

The System Info tab shows the board’s current configuration. The tab displays the contents of the MAX V registers, the JTAG chain, the board’s MAC address, the Qsys memory map, and other details stored on the board.

Figure 16. The System Info Tab

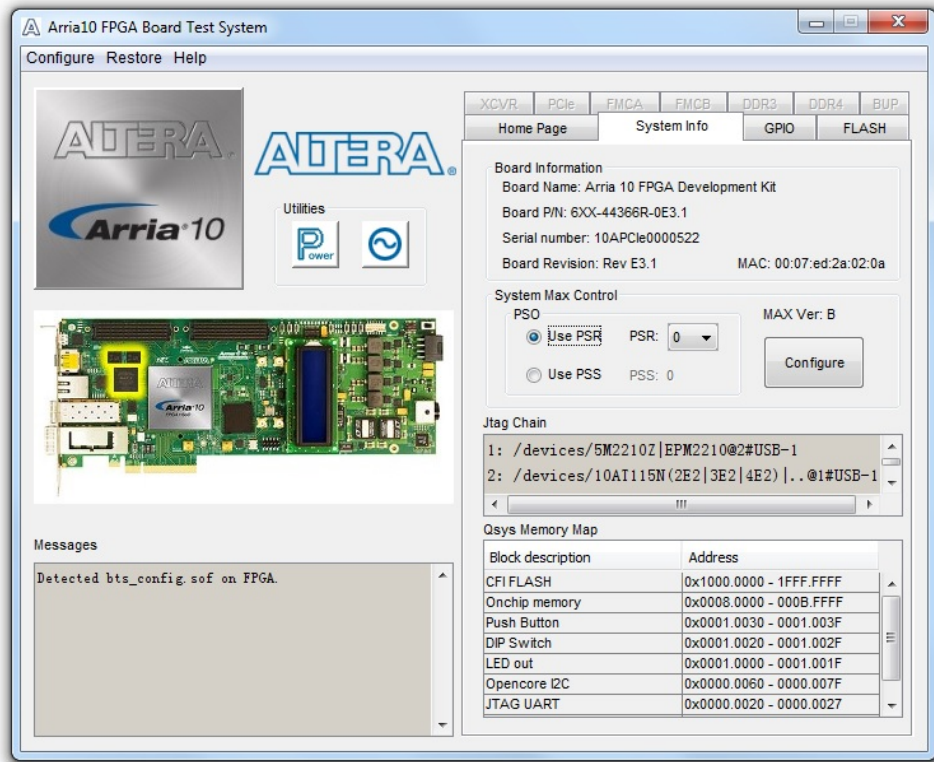


Table 13. Controls on the System Info Tab

| Controls | Description |
|----------------------------|--|
| Board Information Controls | The board information is updated once the GPIO design is configured. Otherwise, this control displays the default static information about your board. |
| Board Name | Indicates the official name of the board, given by the Board Test System. |
| Board P/N | Indicates the part number of the board. |
| Serial Number | Indicates the serial number of the board. |
| Factory Test Version | Indicates the version of the Board Test System currently running on the board. |
| MAC | Indicates the MAC address of the board. |
| MAX V Control | Allows you to view and change the current register values, which take effect immediately: System Reset (SRST) — Write only. Click to reset the FPGA. Page Select Override (PSO) — Read/Write |

continued...

| Controls | Description |
|-----------------|---|
| | Page Select Register (PSR) — Read/Write Page Select Switch (PSS) — Read only MAX Ver: Indicates the version of MAX V code currently running on the board. |
| JTAG Chain | Shows all the devices currently in the JTAG chain. |
| Qsys Memory Map | Shows the memory map of the Qsys system on your board. |

4.4.3. The GPIO Tab

The GPIO tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses.

Figure 17. The GPIO Tab

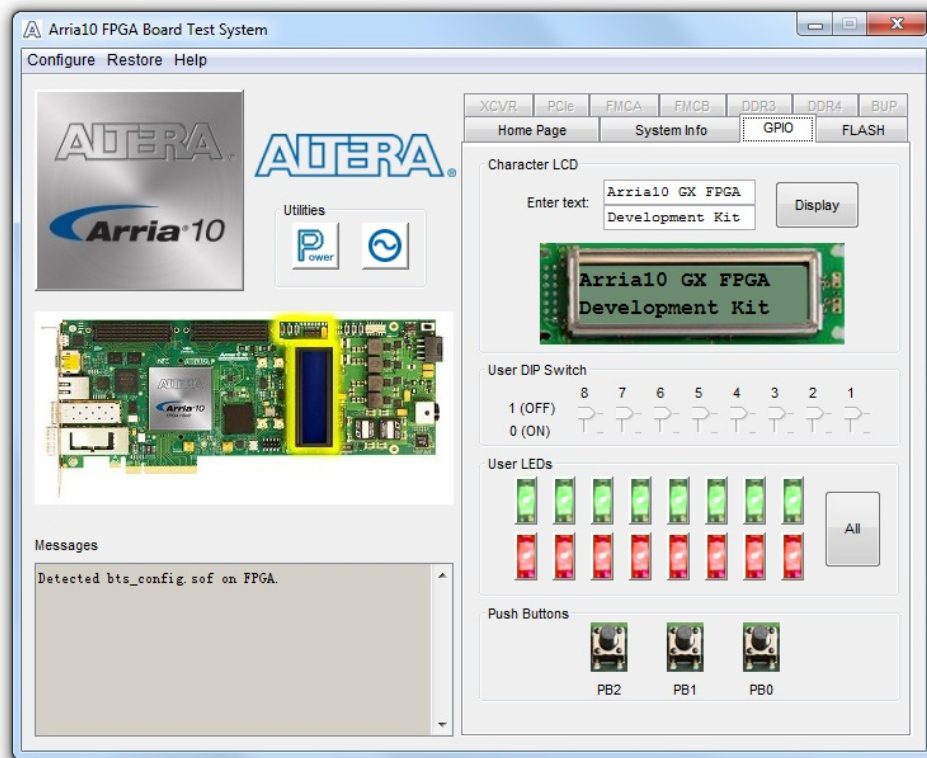


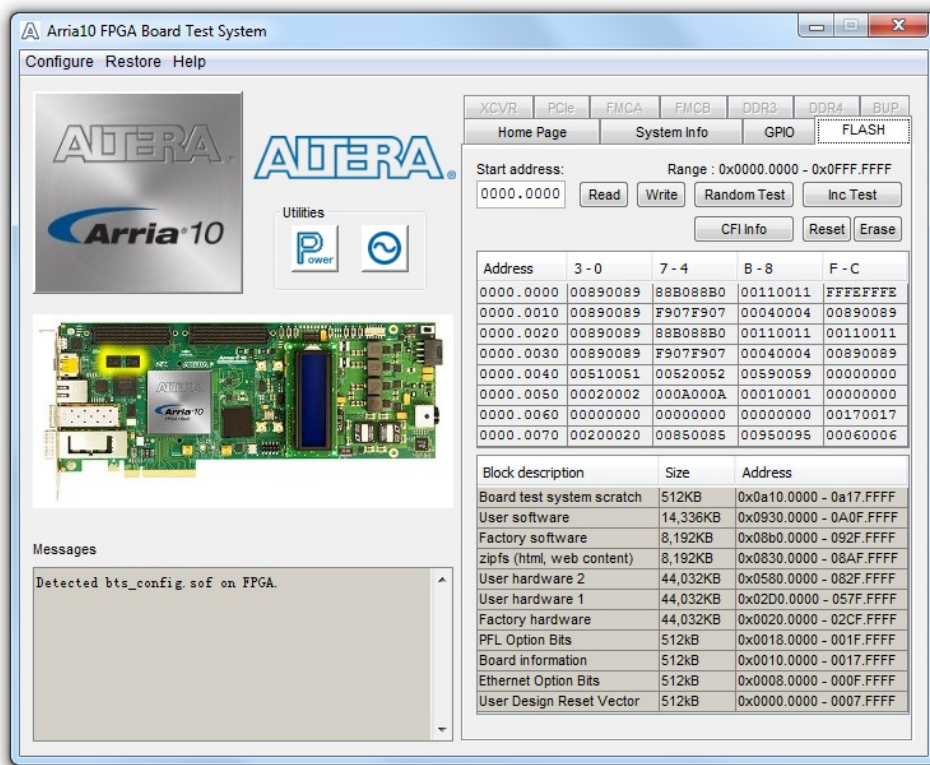
Table 14. Controls on the GPIO Tab

| | |
|----------------------|---|
| Character LCD | Allows you to display text strings on the character LCD on your board. Type text in the text boxes and then click Display . |
| User DIP Switch | Displays the current positions of the switches in the user DIP switch bank (SW2). Change the switches on the board to see the graphical display change accordingly. |
| User LEDs | Displays the current state of the user LEDs for the FPGA. To toggle the board LEDs, click the 0 to 7 buttons to toggle red or green LEDs, or click the All button. |
| Push Button Switches | Read-only control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly. |

4.4.4. The Flash Tab

The **Flash Tab** allows you to read and write flash memory on your board. The memory table will display the CFI ROM table contents by default after you configure the FPGA.

Figure 18. The Flash Tab



| Control | Description |
|----------------|---|
| Read | Reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click Read. Values starting at the specified address appear in the table. |
| Write | Writes the flash memory on your board. To update the flash memory contents, change values in the table and click Write. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents. |
| Random Test | Starts a random data pattern test to flash memory, limited to the 512 K test system scratch page. |
| CFI Query | Updates the memory table, displaying the CFI ROM table contents from the flash device. |
| Increment Test | Starts an incrementing data pattern test to flash memory, limited to the 512 K test system scratch page. |

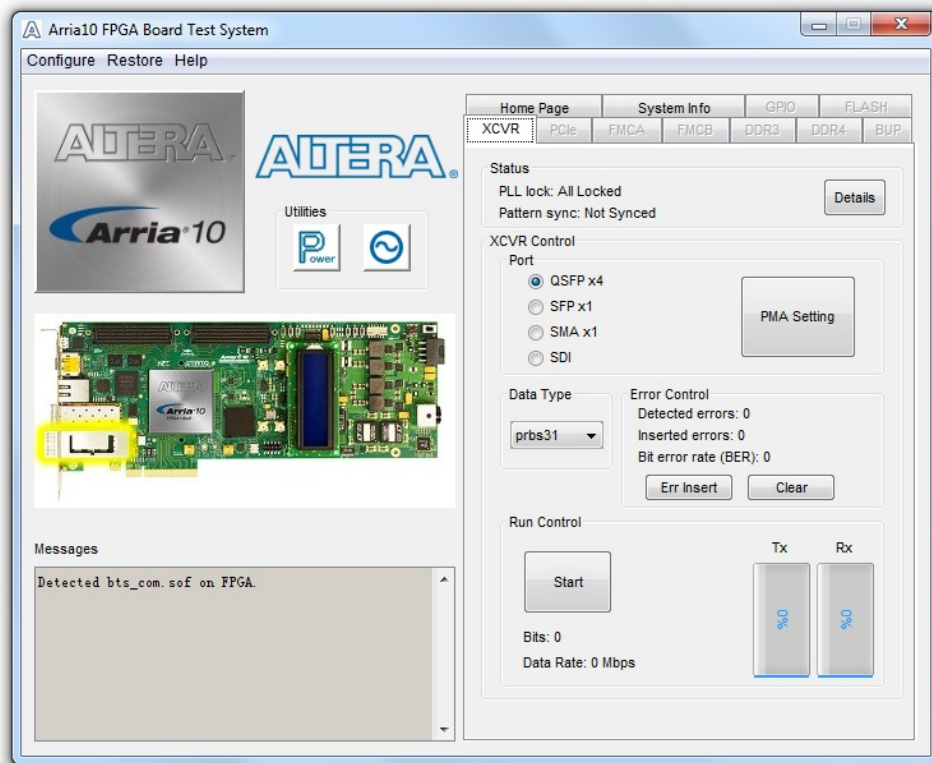
continued...

| Control | Description |
|------------------|---|
| Reset | Executes the flash device's reset command and updates the memory table displayed on the Flash tab. |
| Erase | Erases flash memory. |
| Flash Memory Map | Displays the flash memory map for the development board. |

4.4.5. The XCVR Tab

This tab allows you to perform loopback tests on the QSFP, SFP, SMA, and SDI ports.

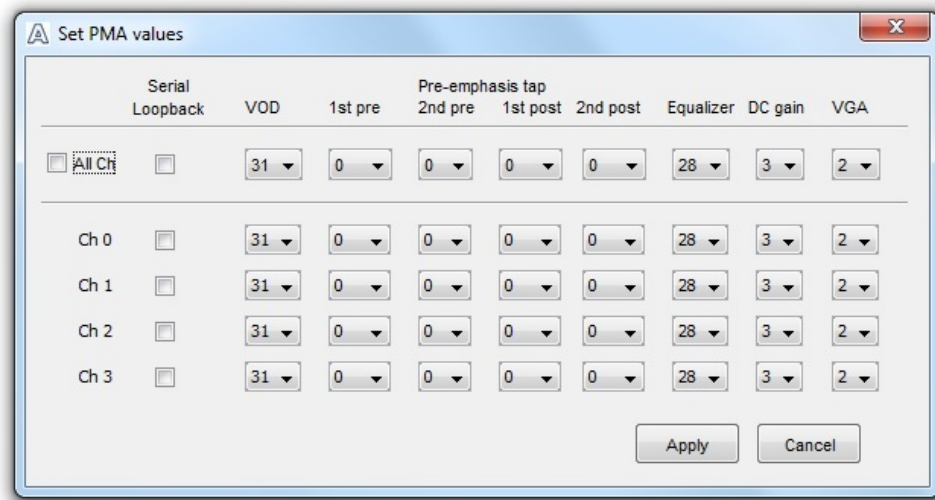
Figure 19. The XCVR Tab



| Control | Description | | | | | | | | | | | | | | | | | | | | |
|---------|---|---------------------|-----------------|---------------------|--------|---|--------|--------|---|---|--------|--------|---|---|--------|--------|---|---|--------|--------|---|
| Status | <p>Displays the following status information during a loopback test:</p> <ul style="list-style-type: none"> PLL lock—Shows the PLL locked or unlocked state. Pattern sync—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected. Details—Shows the PLL lock and pattern sync status: <div data-bbox="581 1423 1409 1753" data-label="Table"> <table border="1"> <thead> <tr> <th>Channel</th> <th>PLL Lock Status</th> <th>Pattern Sync Status</th> <th>Errors</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>1</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>2</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>3</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> </tbody> </table> </div> | Channel | PLL Lock Status | Pattern Sync Status | Errors | 0 | Locked | Synced | 0 | 1 | Locked | Synced | 0 | 2 | Locked | Synced | 0 | 3 | Locked | Synced | 0 |
| Channel | PLL Lock Status | Pattern Sync Status | Errors | | | | | | | | | | | | | | | | | | |
| 0 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 1 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 2 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 3 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| Port | <p>Allows you to specify which interface to test. The following port tests are available:</p> <p style="text-align: right;"><i>continued...</i></p> | | | | | | | | | | | | | | | | | | | | |

| Control | Description |
|---------------|--|
| | QSFP x4 SFP x1 SMA x1 SDI x1 |
| PMA Setting | Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis: Serial Loopback—Routes signals between the transmitter and the receiver. VOD—Specifies the voltage output differential of the transmitter buffer. Pre-emphasis tap <ul style="list-style-type: none"> • 1st pre—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer. • 2nd pre—Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer. • 1st post—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer. • 2nd post—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer. Equalizer—Specifies the AC gain setting for the receiver equalizer in four stage mode. DC gain—Specifies the DC gain setting for the receiver equalizer in four stage mode. VGA—Specifies the VGA gain value. All PMA settings should be changed as in Figure 20 on page 33. |
| Data Type | Specifies the type of data contained in the transactions. The following data types are available for analysis: <ul style="list-style-type: none"> • PRBS 7—Selects pseudo-random 7-bit sequences. • PRBS 15—Selects pseudo-random 15-bit sequences. • PRBS 23—Selects pseudo-random 23-bit sequences. • PRBS 31—Selects pseudo-random 31-bit sequences. • HF—Selects highest frequency divide-by-2 data pattern 10101010. • LF—Selects lowest frequency divide by 33 data pattern. |
| Error Control | Displays data errors detected during analysis and allows you to insert errors: <ul style="list-style-type: none"> • Detected errors—Displays the number of data errors detected in the hardware. • Inserted errors—Displays the number of errors inserted into the transmit data stream. • Insert Error—Inserts a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis. • Clear—Resets the Detected errors and Inserted errors counters to zeroes. |
| Loopback | Start—Initiates the selected ports transaction performance analysis. <i>Note:</i> Always click Clear before Start . Stop—Terminates transaction performance analysis. TX and RX performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve. |

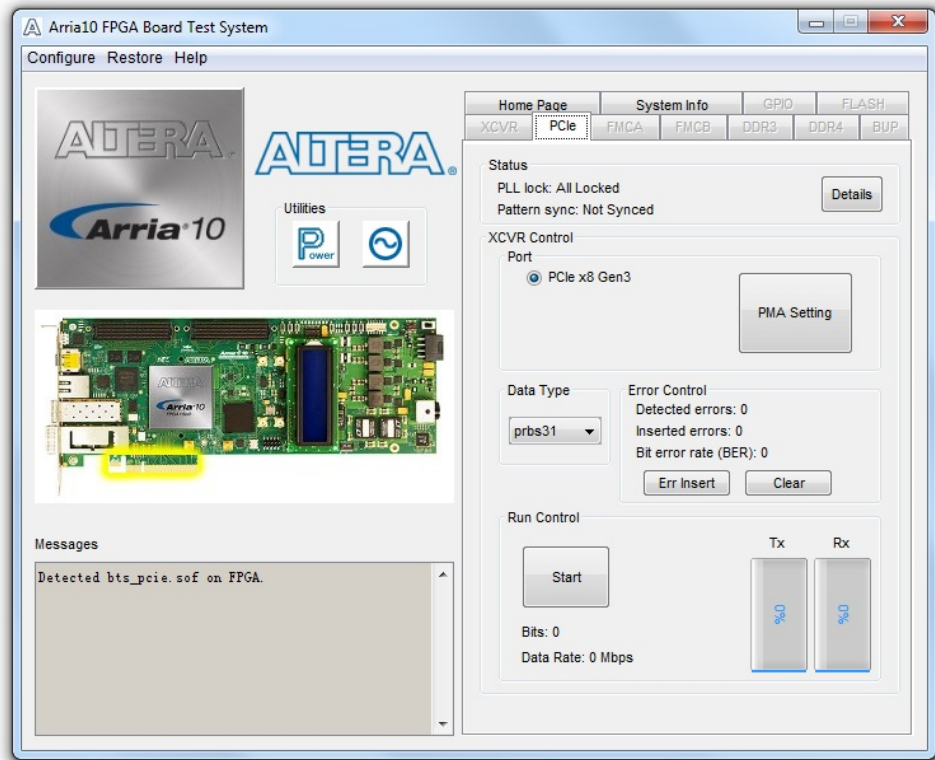
Figure 20. Set PMA Values Window



4.4.6. The PCIe Tab

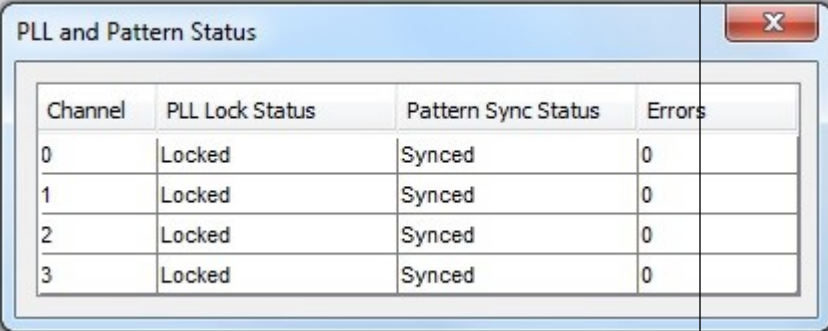
This tab allows you to run a PCIe loopback test on your board. You can also load the design and use an oscilloscope to measure an eye diagram of the PCIe transmit signals.

Figure 21. The PCIe Tab



| Control | Description |
|---------|---|
| Status | Displays the following status information during a loopback test: PLL lock—Shows the PLL locked or unlocked state. Pattern sync—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected. |

continued...

| Control | Description | | | | | | | | | | | | | | | | | | | | |
|---------------|--|---------------------|-----------------|---------------------|--------|---|--------|--------|---|---|--------|--------|---|---|--------|--------|---|---|--------|--------|---|
| | <p>Details—Shows the PLL lock and pattern sync status:</p>  <table border="1" data-bbox="748 422 1533 653"> <thead> <tr> <th>Channel</th> <th>PLL Lock Status</th> <th>Pattern Sync Status</th> <th>Errors</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>1</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>2</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>3</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> </tbody> </table> | Channel | PLL Lock Status | Pattern Sync Status | Errors | 0 | Locked | Synced | 0 | 1 | Locked | Synced | 0 | 2 | Locked | Synced | 0 | 3 | Locked | Synced | 0 |
| Channel | PLL Lock Status | Pattern Sync Status | Errors | | | | | | | | | | | | | | | | | | |
| 0 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 1 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 2 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 3 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| Port | PCIe x8 Gen3 | | | | | | | | | | | | | | | | | | | | |
| PMA Setting | <p>Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:</p> <p>Serial Loopback—Routes signals between the transmitter and the receiver.</p> <p>VOD—Specifies the voltage output differential of the transmitter buffer.</p> <p>Pre-emphasis tap</p> <ul style="list-style-type: none"> 1st pre—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer. 2nd pre—Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer. 1st post—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer. 2nd post—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer. <p>Equalizer—Specifies the AC gain setting for the receiver equalizer in four stage mode.</p> <p>DC gain—Specifies the DC gain setting for the receiver equalizer in four stage mode.</p> <p>VGA—Specifies the VGA gain value.</p> <p>All PMA settings should be changed as in Figure 20 on page 33.</p> | | | | | | | | | | | | | | | | | | | | |
| Data Type | <p>Specifies the type of data contained in the transactions. The following data types are available for analysis:</p> <ul style="list-style-type: none"> PRBS 7—Selects pseudo-random 7-bit sequences. PRBS 15—Selects pseudo-random 15-bit sequences. PRBS 23—Selects pseudo-random 23-bit sequences. PRBS 31—Selects pseudo-random 31-bit sequences. HF—Selects highest frequency divide-by-2 data pattern 10101010. LF—Selects lowest frequency divide by 33 data pattern. | | | | | | | | | | | | | | | | | | | | |
| Error Control | <p>Displays data errors detected during analysis and allows you to insert errors:</p> <ul style="list-style-type: none"> Detected errors—Displays the number of data errors detected in the hardware. Inserted errors—Displays the number of errors inserted into the transmit data stream. Insert Error—Inserts a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis. Clear—Resets the Detected errors and Inserted errors counters to zeroes. | | | | | | | | | | | | | | | | | | | | |
| Loopback | Start—Initiates the selected ports transaction performance analysis. | | | | | | | | | | | | | | | | | | | | |

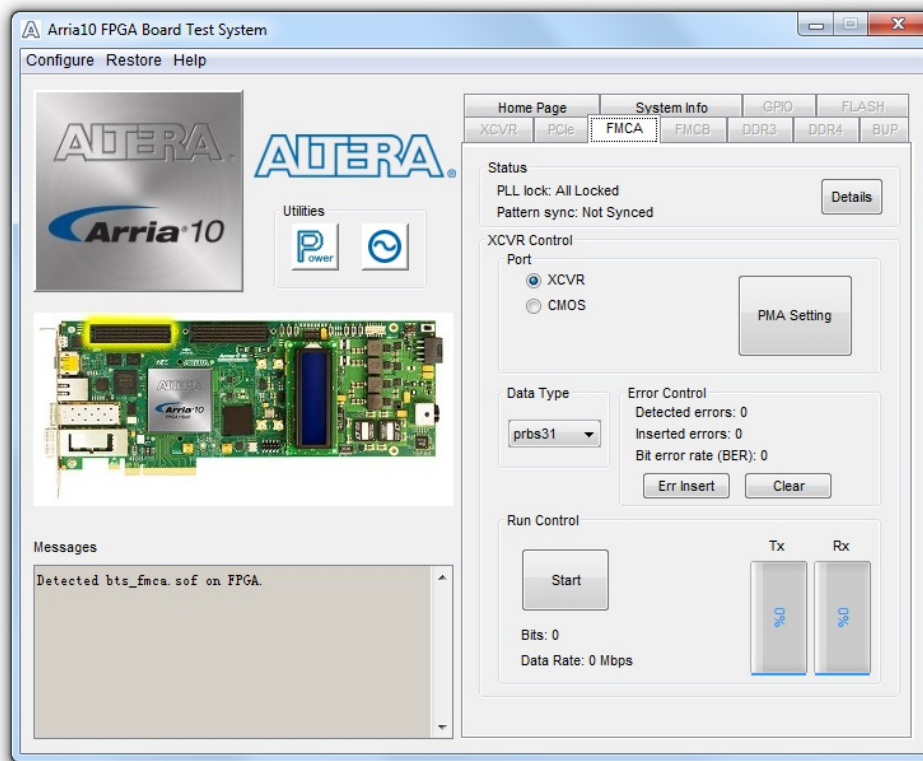
continued...

| Control | Description |
|---------|---|
| | <p><i>Note:</i> Always click Clear before Start.</p> <p>Stop—Terminates transaction performance analysis.</p> <p>TX and RX performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.</p> |

4.4.7. The FMC A Tab

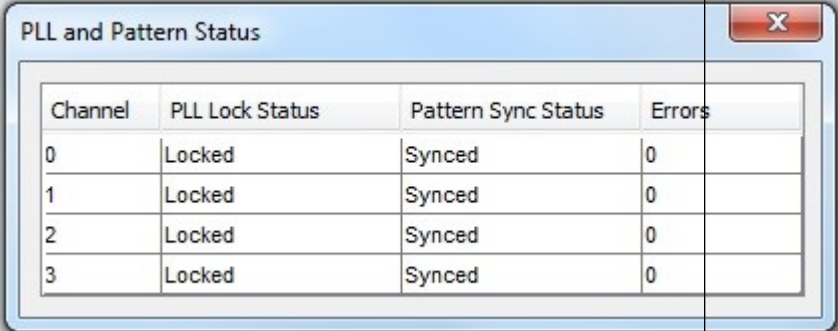
This tab allows you to perform loopback tests on the FMC A port.

Figure 22. The FMC A Tab



| Control | Description |
|---------|---|
| Status | Displays the following status information during a loopback test: PLL lock—Shows the PLL locked or unlocked state. Pattern sync—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected. |

continued...

| Control | Description | | | | | | | | | | | | | | | | | | | | |
|---------------|--|---------------------|-----------------|---------------------|--------|---|--------|--------|---|---|--------|--------|---|---|--------|--------|---|---|--------|--------|---|
| | <p>Details—Shows the PLL lock and pattern sync status:</p>  <table border="1" data-bbox="732 436 1511 653"> <thead> <tr> <th>Channel</th> <th>PLL Lock Status</th> <th>Pattern Sync Status</th> <th>Errors</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>1</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>2</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> <tr> <td>3</td> <td>Locked</td> <td>Synced</td> <td>0</td> </tr> </tbody> </table> | Channel | PLL Lock Status | Pattern Sync Status | Errors | 0 | Locked | Synced | 0 | 1 | Locked | Synced | 0 | 2 | Locked | Synced | 0 | 3 | Locked | Synced | 0 |
| Channel | PLL Lock Status | Pattern Sync Status | Errors | | | | | | | | | | | | | | | | | | |
| 0 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 1 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 2 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| 3 | Locked | Synced | 0 | | | | | | | | | | | | | | | | | | |
| Port | <p>Allows you to specify which interface to test. The following port tests are available:</p> <p>XCVR CMOS</p> | | | | | | | | | | | | | | | | | | | | |
| PMA Setting | <p>Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:</p> <p>Serial Loopback—Routes signals between the transmitter and the receiver.</p> <p>VOD—Specifies the voltage output differential of the transmitter buffer.</p> <p>Pre-emphasis tap</p> <ul style="list-style-type: none"> 1st pre—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer. 2nd pre—Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer. 1st post—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer. 2nd post—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer. <p>Equalizer—Specifies the AC gain setting for the receiver equalizer in four stage mode.</p> <p>DC gain—Specifies the DC gain setting for the receiver equalizer in four stage mode.</p> <p>VGA—Specifies the VGA gain value.</p> <p>All PMA settings should be changed as in Figure 20 on page 33.</p> | | | | | | | | | | | | | | | | | | | | |
| Data Type | <p>Specifies the type of data contained in the transactions. The following data types are available for analysis:</p> <ul style="list-style-type: none"> PRBS 7—Selects pseudo-random 7-bit sequences. PRBS 15—Selects pseudo-random 15-bit sequences. PRBS 23—Selects pseudo-random 23-bit sequences. PRBS 31—Selects pseudo-random 31-bit sequences. HF—Selects highest frequency divide-by-2 data pattern 10101010. LF—Selects lowest frequency divide by 33 data pattern. | | | | | | | | | | | | | | | | | | | | |
| Error Control | <p>Displays data errors detected during analysis and allows you to insert errors:</p> | | | | | | | | | | | | | | | | | | | | |

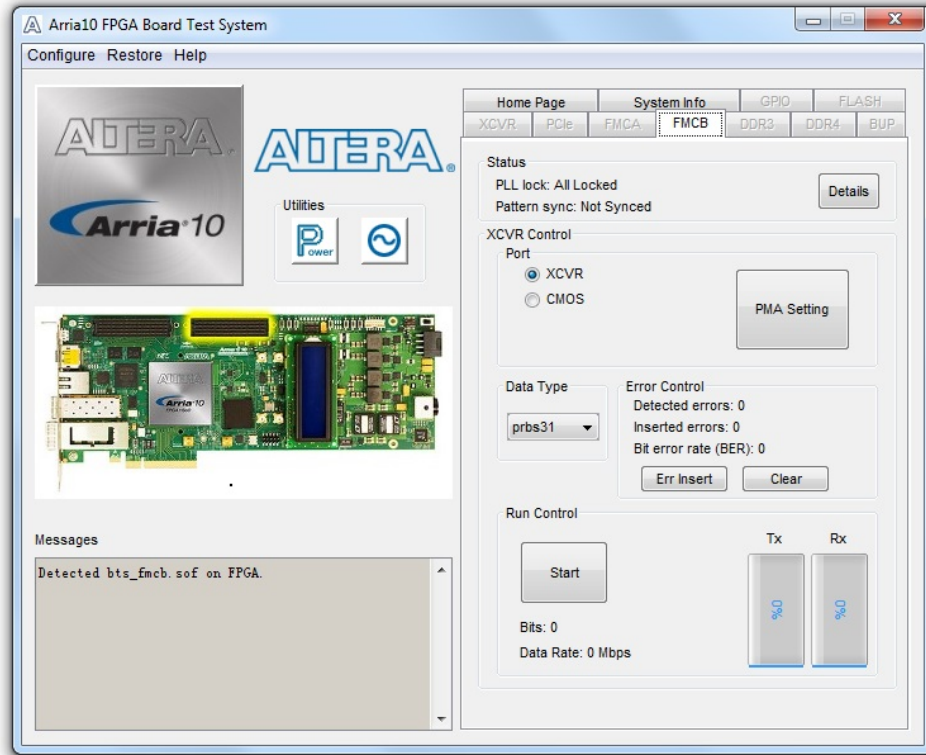
continued...

| Control | Description |
|----------|--|
| | <ul style="list-style-type: none"> • Detected errors—Displays the number of data errors detected in the hardware. • Inserted errors—Displays the number of errors inserted into the transmit data stream. • Insert Error—Inserts a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis. • Clear—Resets the Detected errors and Inserted errors counters to zeroes. |
| Loopback | <p>Start—Initiates the selected ports transaction performance analysis. <i>Note:</i> Always click Clear before Start.</p> <p>Stop—Terminates transaction performance analysis.</p> <p>TX and RX performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.</p> |

4.4.8. The FMC B Tab

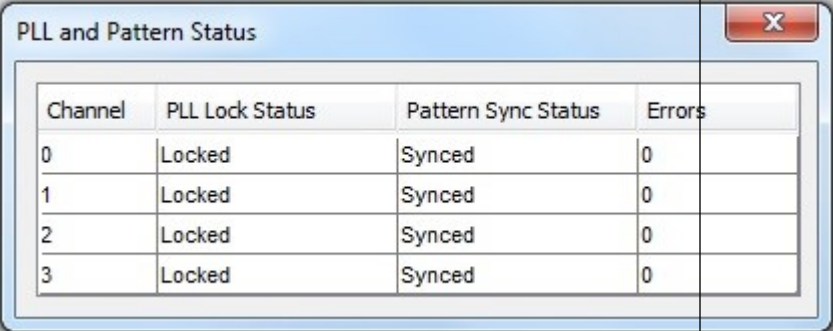
This tab allows you to perform loopback tests on the FMC B port.

Figure 23. The FMC B Tab



| Control | Description |
|---------|---|
| Status | Displays the following status information during a loopback test: PLL lock—Shows the PLL locked or unlocked state. Pattern sync—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected. |

continued...

| Control | Description |
|---------------|--|
| | <p>Details—Shows the PLL lock and pattern sync status:</p>  |
| Port | <p>Allows you to specify which interface to test. The following port tests are available:</p> <p>XCVR CMOS</p> |
| PMA Setting | <p>Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:</p> <p>Serial Loopback—Routes signals between the transmitter and the receiver.</p> <p>VOD—Specifies the voltage output differential of the transmitter buffer.</p> <p>Pre-emphasis tap</p> <ul style="list-style-type: none"> • 1st pre—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer. • 2nd pre—Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer. • 1st post—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer. • 2nd post—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer. <p>Equalizer—Specifies the AC gain setting for the receiver equalizer in four stage mode.</p> <p>DC gain—Specifies the DC gain setting for the receiver equalizer in four stage mode.</p> <p>VGA—Specifies the VGA gain value.</p> <p>All PMA settings should be changed as in Figure 20 on page 33.</p> |
| Data Type | <p>Specifies the type of data contained in the transactions. The following data types are available for analysis:</p> <ul style="list-style-type: none"> • PRBS 7—Selects pseudo-random 7-bit sequences. • PRBS 15—Selects pseudo-random 15-bit sequences. • PRBS 23—Selects pseudo-random 23-bit sequences. • PRBS 31—Selects pseudo-random 31-bit sequences. • HF—Selects highest frequency divide-by-2 data pattern 10101010. • LF—Selects lowest frequency divide by 33 data pattern. |
| Error Control | <p>Displays data errors detected during analysis and allows you to insert errors:</p> |

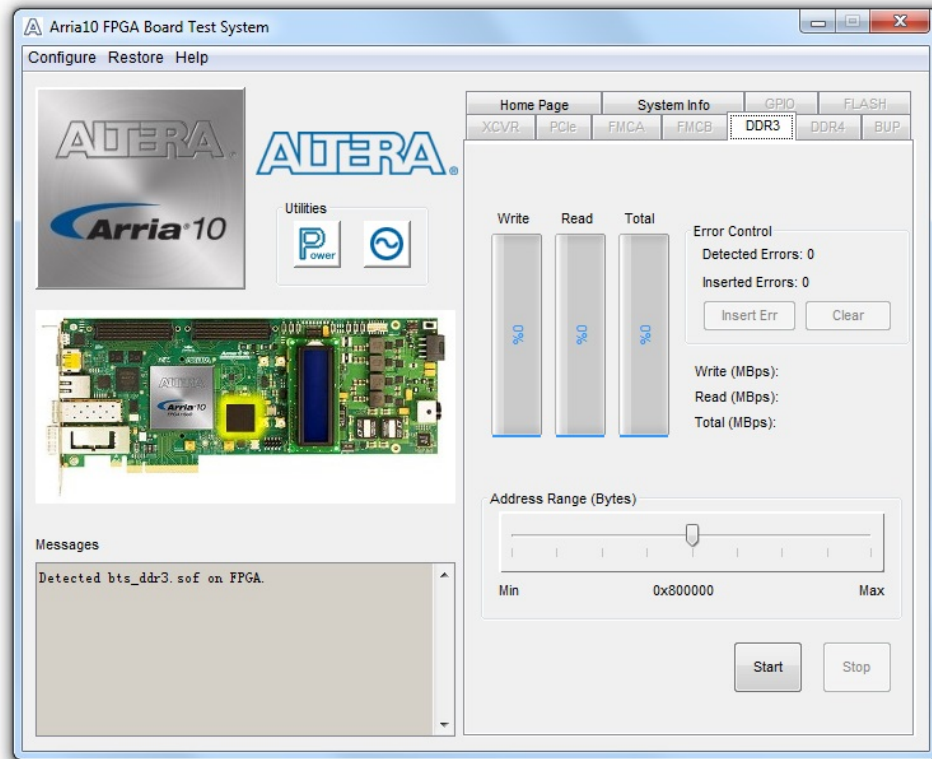
continued...

| Control | Description |
|----------|--|
| | <ul style="list-style-type: none"> • Detected errors—Displays the number of data errors detected in the hardware. • Inserted errors—Displays the number of errors inserted into the transmit data stream. • Insert Error—Inserts a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis. • Clear—Resets the Detected errors and Inserted errors counters to zeroes. |
| Loopback | <p>Start—Initiates the selected ports transaction performance analysis. <i>Note:</i> Always click Clear before Start.</p> <p>Stop—Terminates transaction performance analysis.</p> <p>TX and RX performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.</p> |

4.4.9. The DDR3 Tab

This tab allows you to read and write DDR3 memory on your board.

Figure 24. The DDR3 Tab



| Control | Description |
|------------------------|--|
| Start | Initiates DDR3 memory transaction performance analysis. |
| Stop | Terminates transaction performance analysis. |
| Performance Indicators | <p>These controls display current transaction performance analysis information collected since you last clicked Start:</p> <ul style="list-style-type: none"> • Write, Read, and Total performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve. • Write (MBps), Read (MBps), and Total (MBps)—Show the number of bytes of data analyzed per second. • Data bus: 72 bits (8 bits ECC) wide and the frequency is 1066 MHz double data rate. 2133 Megabits per second (Mbps) per pin. Equating to a theoretical maximum bandwidth of 136512 Mbps or 17064 MBps. |
| Error Control | This control displays data errors detected during analysis and allows you to insert errors: |

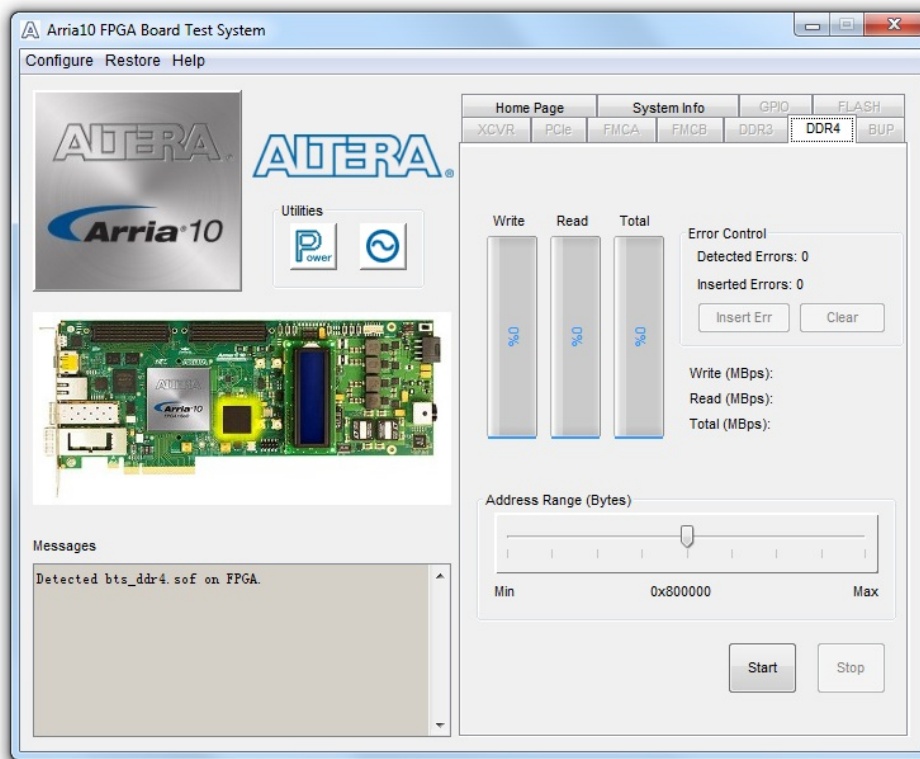
continued...

| Control | Description |
|---------------------------------------|--|
| | <ul style="list-style-type: none"> • Detected errors—Displays the number of data errors detected in the hardware. • Inserted errors—Displays the number of errors inserted into the transaction stream. • Insert Error—Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis. • Clear—Resets the Detected errors and Inserted errors counters to zeroes. |
| Number of Addresses to Write and Read | Determines the number of addresses to use in each iteration of reads and writes. |

4.4.10. The DDR4 Tab

This tab allows you to read and write DDR4 memory on your board.

Figure 25. The DDR4 Tab



| Control | Description |
|------------------------|--|
| Start | Initiates DDR4 memory transaction performance analysis. |
| Stop | Terminates transaction performance analysis. |
| Performance Indicators | <p>These controls display current transaction performance analysis information collected since you last clicked Start:</p> <ul style="list-style-type: none"> • Write, Read, and Total performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve. • Write (MBps), Read (MBps), and Total (MBps)—Show the number of bytes of data analyzed per second. • Data bus: 72 bits (8 bits ECC) wide and the frequency is 1066 MHz double data rate. 2133 Megabits per second (Mbps) per pin. Equating to a theoretical maximum bandwidth of 136512 Mbps or 17064 MBps. |
| Error Control | This control displays data errors detected during analysis and allows you to insert errors: |

continued...

| Control | Description |
|---------------------------------------|--|
| | <ul style="list-style-type: none"> • Detected errors—Displays the number of data errors detected in the hardware. • Inserted errors—Displays the number of errors inserted into the transaction stream. • Insert Error—Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis. • Clear—Resets the Detected errors and Inserted errors counters to zeroes. |
| Number of Addresses to Write and Read | Determines the number of addresses to use in each iteration of reads and writes. |

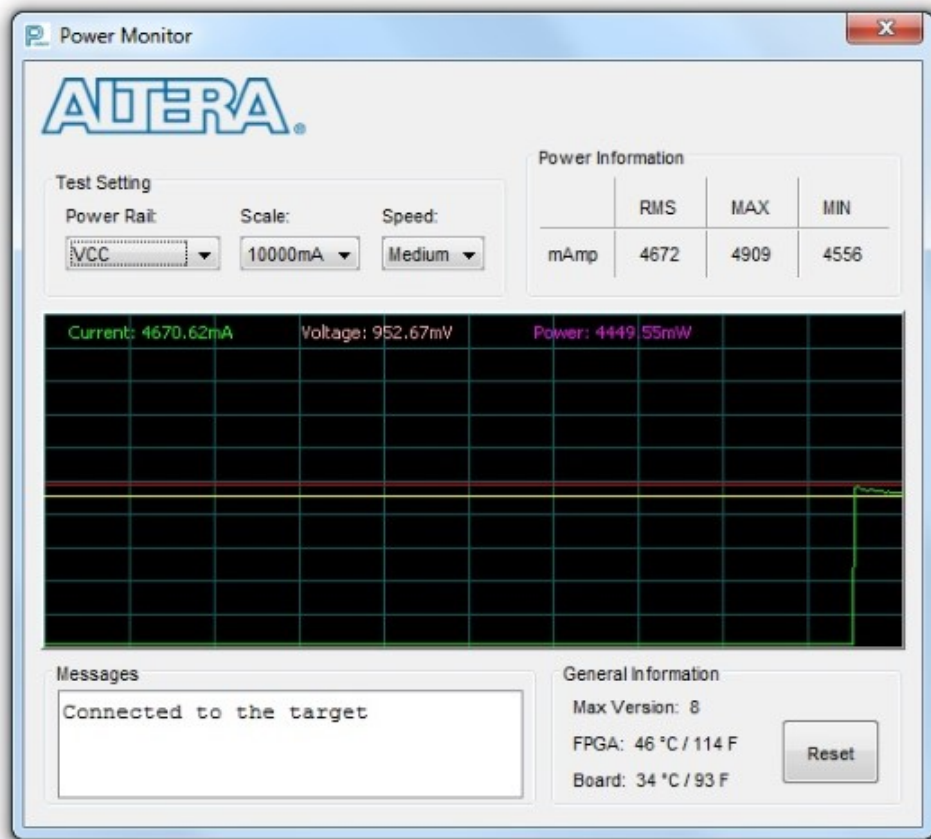
4.4.11. The Power Monitor

The Power Monitor measures and reports current power information and communicates with the MAX V device on the board through the JTAG bus. A power monitor circuit attached to the MAX V device allows you to measure the power that the FPGA is consuming.

To start the application, click the Power Monitor icon in the Board Test System application. You can also run the Power Monitor as a stand-alone application. The PowerMonitor.exe resides in the <package dir>\examples\board_test_system directory.

Note: You cannot run the stand-alone power application and the BTS application at the same time. Also, you cannot run power and clock interface at the same time

Figure 26. Power Monitor Interface



| Control | Description |
|---------------|---|
| Test Settings | Displays the following controls: Power Rail —Indicates the currently-selected power rail. After selecting the desired rail, click Reset to refresh the screen with updated board readings. |

continued...

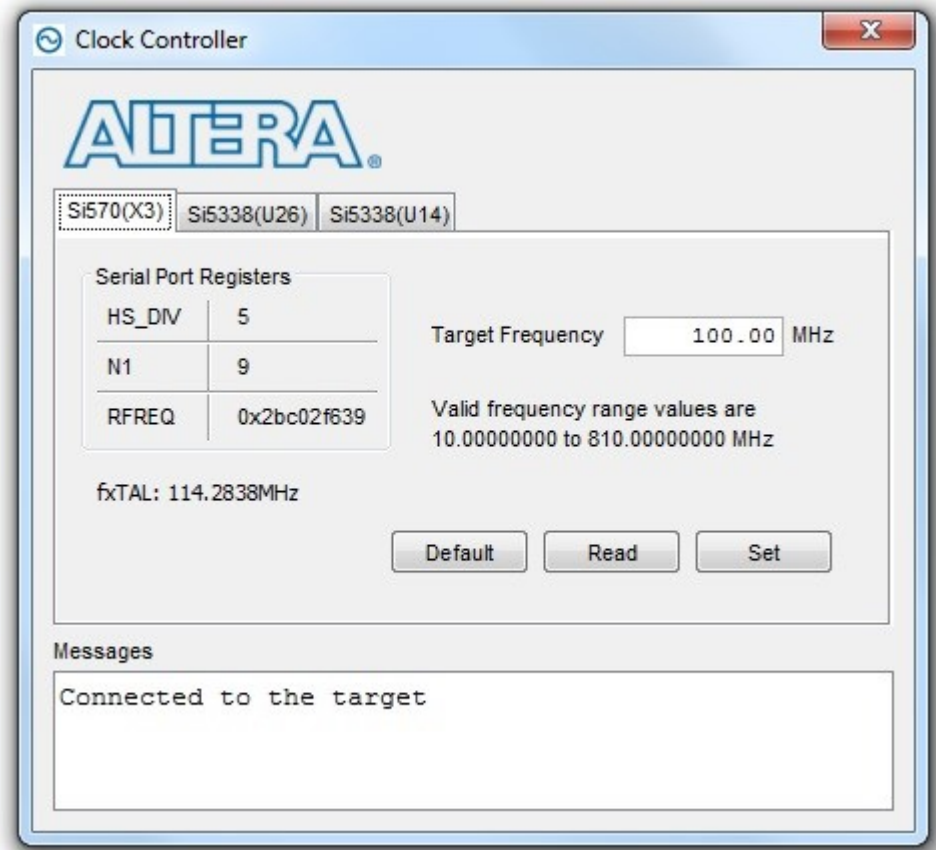
| Control | Description |
|---------------------|---|
| | <p>Scale—Specifies the amount to scale the power graph. Select a smaller number to zoom in to see finer detail. Select a larger number to zoom out to see the entire range of recorded values.</p> <p>Speed—Specifies how often to refresh the graph.</p> |
| Power Information | Displays root-mean-square (RMS) current, maximum, and minimum numerical power readings in mA. |
| Graph | Displays the mA power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset. |
| General Information | Displays MAX V version and current temperature of the FPGA and board. |
| Reset | Clears the graph, resets the minimum and maximum values, and restarts the Power Monitor. |

4.4.12. The Clock Control

The Clock Control application set the three programmable oscillators to any frequency between 10 MHz and 810 MHz. The frequencies support eight digits of precision to the right of the decimal point.

The Clock Control communicates with the MAX V device on the board through the JTAG bus. The programmable oscillators are connected to the MAX V device through a 2-wire serial bus.

Figure 27. Si570 (X3) Tab



| Control | Description |
|------------------------|--|
| Serial Port Registers | Shows the current values from the Si570 registers for frequency configuration. |
| Target frequency (MHZ) | Allows you to specify the frequency of the clock. Legal values are between 10 and 810 MHz with eight digits of precision to the right of the decimal point. For example, 421.31259873 is possible within 100 parts per million (ppm). The Target frequency control works in conjunction with the Set New Freq control. |

continued...

| Control | Description |
|--------------|--|
| FXTAL | Shows the calculated internal fixed-frequency crystal, based on the serial port register values. |
| Default | Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board. |
| Set New Freq | Sets the programmable oscillator frequency for the selected clock to the value in the Target frequency control for the programmable oscillators. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies. |

Each Si5338 tab for U26 and U14 display the same GUI controls for each clock generators. Each tab allows for separate control. The Si5338 is capable of synthesizing four independent user-programmable clock frequencies up to 350 MHz and select frequencies up to 710 MHz.

Figure 28. Si5338 (U26) Tab

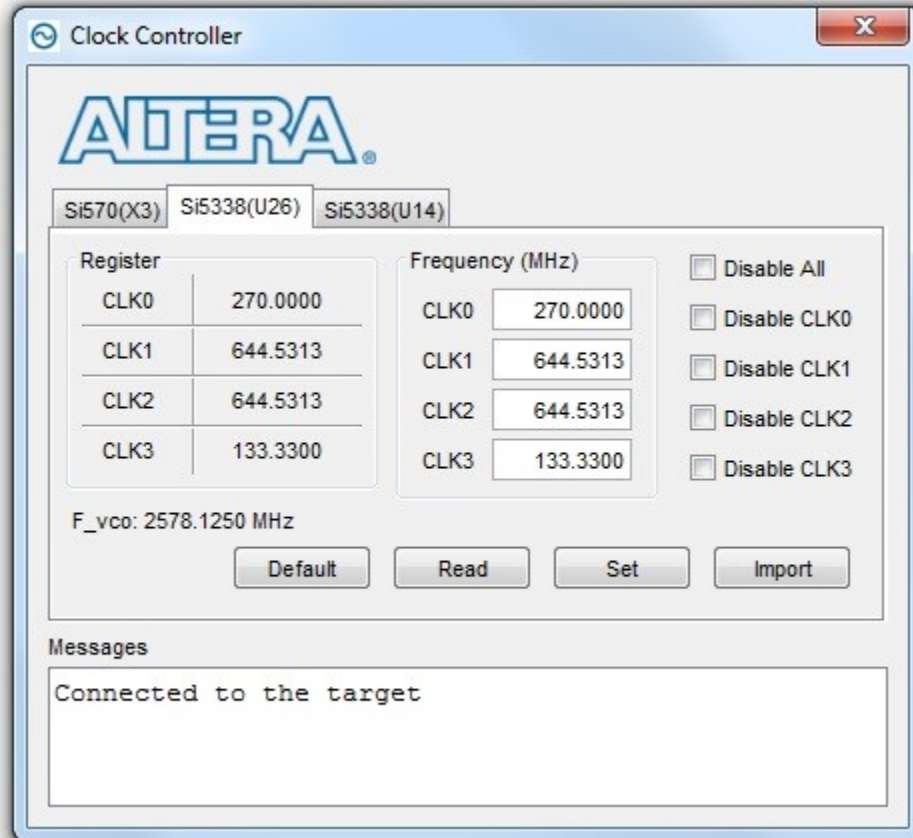
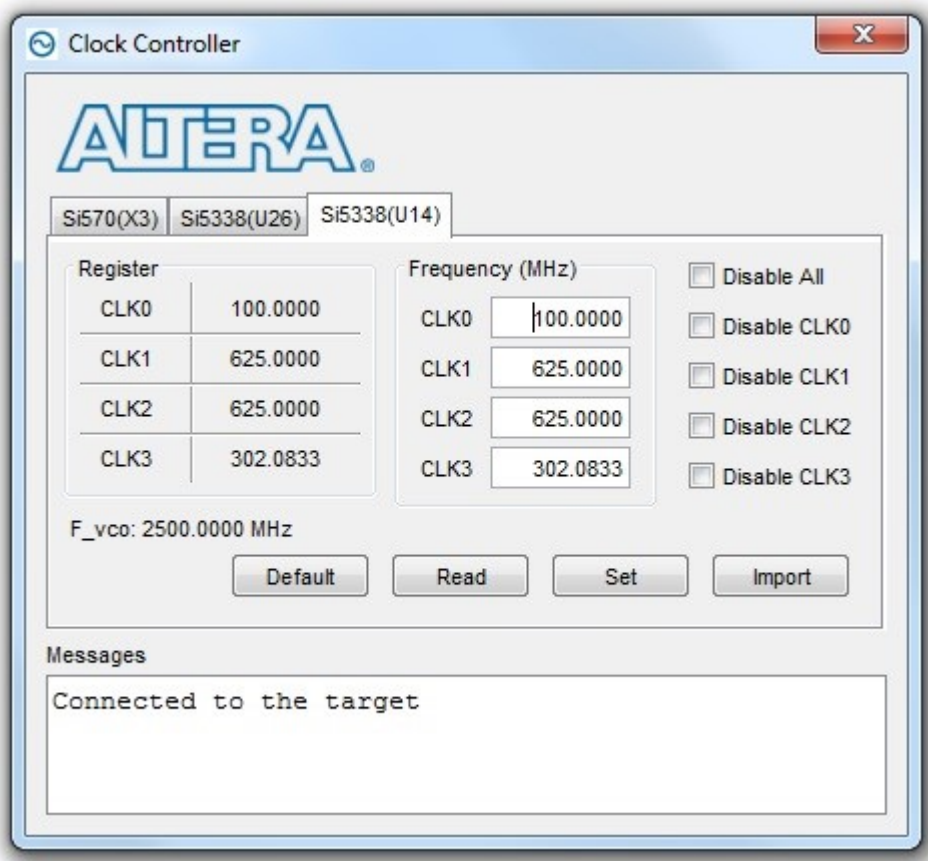


Figure 29. Si5338 (U14) Tab



| Control | Description |
|-----------------|--|
| F_vco | Displays the generating signal value of the voltage-controlled oscillator. |
| Registers | Display the current frequencies for each oscillator. |
| Frequency (MHz) | Allows you to specify the frequency of the clock. |
| Disable all | Disable all oscillators at once. |
| Read | Reads the current frequency setting for the oscillator associated with the active tab. |
| Default | Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board. |
| Set New Freq | Sets the programmable oscillator frequency for the selected clock to the value in the CLK0 to CLK3 controls for the Si5338 (U26 and U14). Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies. |
| Import Reg Map | Import register map file generated from Silicon Laboratories ClockBuilder Desktop. |

5. Board Update Portal

The Arria 10 GX FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with SW6.4 FACTORY_LOAD in the default position, the Arria 10 GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user portion of the flash memory and provides links to useful information on the Altera website, including kit-specific links and design resources.

After successfully updating the user flash memory, you can load the user design from the flash memory into the FPGA. To do so, set SW6.4 to OFF position and power cycle the board.

The source code for the Board Update Portal design resides in the `<package dir>\examples\board_update_portal` directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to the "Factory Reset" section for information on how to restore the boards original factory contents.

Related Information

[Factory Reset](#) on page 18

5.1. Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page. Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet cable, power cables, and development board that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. Install the latest Altera software tools, including the Quartus Prime software, Nios II processor and IP functions. If necessary, download the Quartus Prime Lite Edition software.
2. With the board powered down, set SW6.4 to the ON position.
3. Attach the Ethernet cable from the board to your LAN.
4. Power up the board. The board connects to the LAN's gateway router and obtains an IP address. The LCD on the board will display the IP address.
5. Launch a web browser on the PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page will appear in the browser.

You can click Arria 10 GX FPGA Development Kit on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the Arria 10 GX FPGA Development Kit page of the Altera website to determine if you have the latest kit software.

Related Information

- [Quartus Prime Software Page](#)
- [Arria 10 GX FPGA Development Kit Web Page](#)

5.1.1. Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user portion of the flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Arria 10 GX FPGA Development Kit page include **.flash** files. You can also create **.flash** files from your own custom designs.

To upload a design over the network into the user portion of the flash memory on your board, perform the following steps:

1. Perform the steps in “Connecting to the Board Update Portal Web Page” section to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field or otherwise leave the field blank.
3. Click **Upload**. The progress bar indicates the percent complete. The file will take about 20 seconds to upload.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set SW6.4 to the OFF position.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user portion of the flash memory. If you do overwrite the factory image, you can restore it by following the instructions in the “Factory Reset” section.

Related Information

[Factory Reset](#) on page 18

6. Board Components

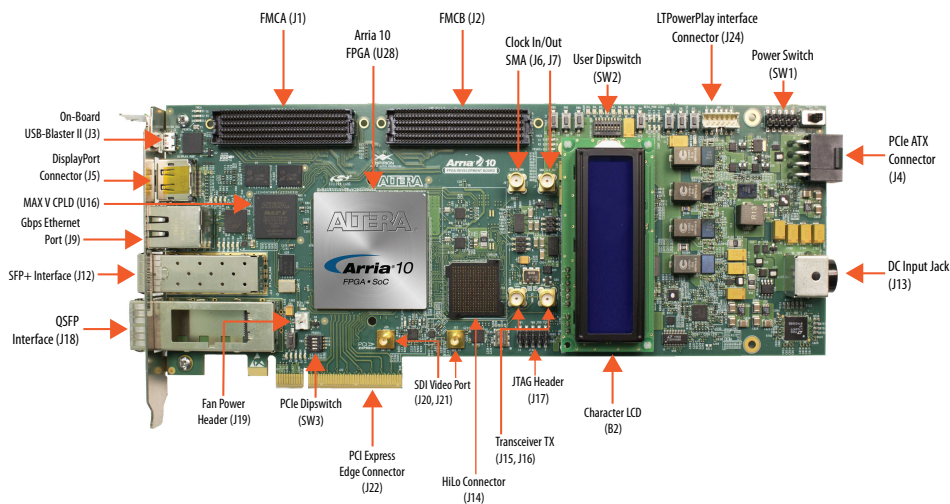
This chapter introduces all the important components on the development kit board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the development kit documents directory.

6.1. Board Overview

This section provides an annotated board image and the major component descriptions.

Figure 30. Overview of the Development Board Features (ES Edition)



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*Other names and brands may be claimed as the property of others.

Figure 31. Overview of the Development Board Features

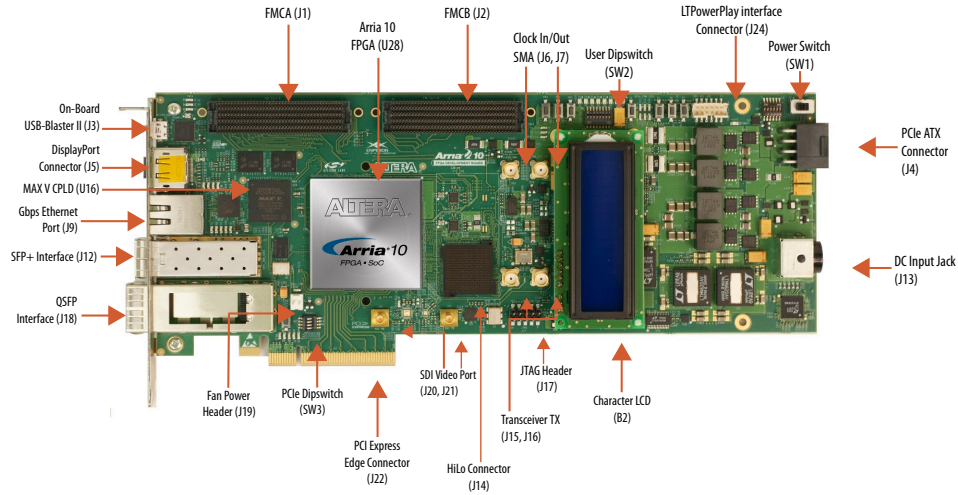


Table 15. Arria 10 GX FPGA Development Board Components

| Board Reference | Type | Description |
|---|--------------------------------|--|
| Featured Devices | | |
| U28 | FPGA | Arria 10 GX FPGA, 10AX115S2F45I1SG: <ul style="list-style-type: none"> Adaptive logic modules (ALMs): 427,200 LEs (K): 1,150 Registers: 1,708,800 M20K memory blocks: 2,713 Transceiver count: 96 Package Type: 1932 BGA |
| U16 | CPLD | MAX V CPLD, 2210 LEs, 256FBGA 1.8V VCCINT |
| Board Reference | Type | Description |
| Configuration and Setup Elements | | |
| J3 | On-Board USB-Blaster II | Micro-USB 2.0 connector for programming and debugging the FPGA. |
| SW3 | PCI Express Control DIP switch | Enables PCI Express link widths x1, x4, and x8. |
| SW4 | JTAG Bypass DIP switch | Enables and disables devices in the JTAG chain. This switch is located on the back of the board. |
| SW5 | FPP Configuration DIP Switch | Sets the Arria 10 MSEL pins and VID_EN pin. |
| SW6 | Board settings DIP switch | Controls the MAX V CPLD System Controller functions such as clock select, clock enable, factory or user design load from flash and FACTORY signal command sent at power up. This switch is located at the bottom of the board. |
| S4 | CPU reset push button | The default reset for the FPGA logic. |
| <i>continued...</i> | | |

| Board Reference | Type | Description |
|---|-----------------------------------|--|
| Configuration and Setup Elements | | |
| S5 | Image select push button | Toggles the configuration LEDs which selects the program image that loads from flash memory to the FPGA. |
| S6 | Program configuration push button | Configures the FPGA from flash memory image based on the program LEDs. |
| S7 | MAX V reset push button | The default reset for the MAX V CPLD System Controller. |

| Board Reference | Type | Description |
|---------------------------------|------------------------|--|
| Status Elements | | |
| D22, D23 | JTAG LEDs | Indicates transmit or receive activity of the JTAG chain. The TX and RX LEDs flicker if the link is in use and active. |
| D24, D25 | System Console LEDs | Indicates the transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle. |
| D12, D13, D14 | Program LEDs | Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the program load push button. |
| D17 | Configuration done LED | Illuminates when the FPGA is configured. |
| D15 | Load LED | Illuminates during FPGA configuration. |
| D16 | Error LED | Illuminates when the FPGA configuration from flash fails. |
| D19 | Power LED | Illuminates when the board is powered on. |
| D32 | Temperature LED | Illuminates when an over temperature condition occurs for the FPGA device. Ensure that an adequate heatsink/fan is properly installed.. |
| D26, D27, D28, D29, D30 | Ethernet LEDs | Shows the connection speed as well as transmit or receive activity. |
| D33 | SDI Cable LED | Illuminates to show the transmit or receive activity. |
| D34, D35, D36, D37, D38 | PCI Express link LEDs | You can configure these LEDs to display the PCI Express link width (x1, x4, x8) and data rate. |
| D3, D4, D5, D6, D7, D8, D9, D10 | User defined LEDs | Eight bi-color LEDs (green and red) for 16 user LEDs. Illuminates when driven low. |
| D1, D2, D11 | FMCA LEDs | Illuminates for RX, TX, PRSNTn activity. |
| D18, D20, D21 | FMCB LEDs | Illuminates for RX, TX, PRSNTn activity. |

| Board Reference | Type | Description |
|------------------------|-------------------------|--|
| Clock Circuitry | | |
| X1 | SDI reference clock | SW6.3 DIP switch controlled: FS=0: 148.35 MHz FS=1: 148.50 MHz |
| X3 | Programmable oscillator | Si570 programmable oscillator by the clock control GUI. Default is 100 MHz. |
| X2 | 125.0-MHz oscillator | 125.0-MHz voltage controlled crystal oscillator for the Ethernet interface.. |
| <i>continued...</i> | | |

| Board Reference | Type | Description |
|------------------------|---|---|
| Clock Circuitry | | |
| X4 | 50-MHz oscillator | 50.000-MHz crystal oscillator for general purpose logic. |
| U26 | Quad-output oscillator | Si5338 programmable oscillator for clock control GUI. (Defaults CLK[0:3] = 270MHz, 644.53125MHz, 644.53125MHz, 133.33MHz) |
| U14 | Quad-output oscillator | Si5338 programmable oscillator for clock control GUI. (Defaults CLK[0:3] = 100MHz, 625MHz, 625MHz, 302.083333MHz) |
| J6 | Clock input SMA connector | Signal: CLKIN_SMA |
| J7 | Clock output SMA connector | Signal: SMA_CLK_OUT |
| J20, J21 | SDI (Serial Digital Interface) transceiver connectors | Two sub-miniature version B (SMB) connectors. Drives serial data input/output to or from SDI video port. |

| Board Reference | Type | Description |
|-------------------------------|---------------|--|
| Transceiver Interfaces | | |
| J15 | SMA connector | SMA_TX_N from the left transceiver bank - 1H |
| J16 | SMA connector | SMA_TX_P from the left transceiver bank - 1H |

| Board Reference | Type | Description |
|----------------------------------|---------------------------|--|
| General User Input/Output | | |
| SW2 | FPGA user DIP switch | Octal user DIP switches. When the switch is ON, a logic 0 is selected. |
| S1, S2, S3 | General user push buttons | Three user push buttons. Driven low when pressed. |
| D3, D4, D5, D6, D7, D8, D9, D10 | User defined LEDs | Eight bi-color user LEDs. Illuminates when driven low. |

| Board Reference | Type | Description |
|-----------------------|----------------|---|
| Memory Devices | | |
| J14 | HiLo Connector | One x72 memory interface supporting DDR3 (x72), DDR4 (x72), QDR4 (x36), and RLDRAM 3 (x36). This development kit includes three plugin modules (daughtercards) that use the HiLo connector: <ul style="list-style-type: none"> • DDR4 memory (x72) 1200 MHz • DDR3 memory (x72) 1066 MHz, Ping Pong PHY. • RLDRAM3 memory (x36) 1,200 MHz |
| U4, U5 | Flash memory | ICS - 1GBIT STRATA FLASH, 16-BIT DATA, VCC=VCCQ=1.7V-2.0V, 64-BALL EASY BGA (10MM X 8MM) |

| Board Reference | Type | Description |
|----------------------------|-------------------------------|---|
| Communication Ports | | |
| J22 | PCI Express x8 edge connector | Made of gold-plated edge fingers for up to x8 signaling in either Gen1, Gen2, or Gen3 mode. |
| J1, J2 | FMC Port | FPGA mezzanine card ports A and B. |

continued...

| Board Reference | Type | Description |
|----------------------------|-------------------------------|---|
| Communication Ports | | |
| J9 | Gbps Ethernet RJ-45 connector | RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MAC MegaCore function in SGMII mode. |
| J18 | QSFP interface | Provides four transceiver channels for a 40G QSFP module. |
| J12 | SFP+ connector | SFP+ XCVR interface. |
| J3 | Micro-USB connector | Embedded Altera USB-Blaster II JTAG for programming the FPGA via a USB cable. |

| Board Reference | Type | Description |
|----------------------|-----------------------|--|
| Display Ports | | |
| J5 | DisplayPort connector | Molex 0.50mm pitch DisplayPort male receptacle, right angle, surface mount, 0.76µm gold plating, 20 circuits with cover. |
| B2 | Character LCD | Connector which interfaces to the provided 16 character × 2 line LCD module. |
| J20, J21 | SDI video port | Two sub-miniature version B (SMB) connectors that provide a full-duplex SDI interface. |

| Board Reference | Type | Description |
|---------------------|------------------------------|--|
| Power Supply | | |
| J22 | PCI Express edge connector | Interfaces to a PCI Express root port such as an appropriate PC motherboard. |
| J13 | DC input jack | Accepts a 12-V DC power supply. Do not use this input jack while the board is plugged into a PCI Express slot. |
| SW1 | Power Switch | Switch to power on or off the board when power is supplied from the DC input jack. |
| J4 | PCIe 2x4 ATX power connector | 12-V ATX input. This input must be connected when the board is plugged into a PCIe root port. |

6.2. MAX V CPLD System Controller

The board utilizes the EPM2210 System Controller, an Altera MAX V CPLD, for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Temperature monitoring
- Fan control
- Control registers for clocks
- Control registers for remote update system

Table 16. MAX V CPLD System Controller Device Pin-Out

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|---|
| CLK125_EN | E9 | 2.5 V | 125 MHz oscillator enable |
| CLK50_EN | J16 | 1.8 V | 50 MHz oscillator enable |
| CLK_CONFIG | J5 | 1.8 V | Clock Configure |
| CLK_ENABLE | D4 | 2.5 V | Clock Enable |
| CLK_SEL | A2 | 2.5 V | Clock Select |
| CLOCK_I2C_SCL | C12 | 2.5 V | Serial clock line for I ² C |
| CLOCK_I2C_SDA | C10 | 2.5 V | Serial data line for I ² C |
| CPU_RESETN | K4 | 1.8 V | FPGA reset push button |
| FACTORY_LOAD | B5 | 2.5 V | DIP switch to load factory or user design at power-up |
| FLASH_ADVN | N14 | 1.8 V | FSM bus flash memory address valid |
| FLASH_CEN0 | D14 | 1.8 V | FSM bus flash memory chip enable |
| FLASH_CEN1 | F11 | 1.8 V | FSM bus flash memory chip enable |
| FLASH_CLK | N15 | 1.8 V | FSM bus flash memory clock |
| FLASH_OEN | P14 | 1.8 V | FSM bus flash memory output enable |
| FLASH_RDYBSYN0 | F12 | 1.8 V | FSM bus flash memory ready |
| FLASH_RDYBSYN1 | P15 | 1.8 V | FSM bus flash memory ready |
| FLASH_RESETN | D13 | 1.8 V | FSM bus flash memory reset |
| FLASH_WEN | J1 | 1.8 V | FSM bus flash memory write enable |
| FM_A1 | F15 | 1.8 V | FM address bus |
| FM_A2 | G16 | 1.8 V | FM address bus |
| FM_A3 | G15 | 1.8 V | FM address bus |
| FM_A4 | H16 | 1.8 V | FM address bus |
| FM_A5 | H15 | 1.8 V | FM address bus |
| FM_A6 | F16 | 1.8 V | FM address bus |
| FM_A7 | G14 | 1.8 V | FM address bus |
| FM_A8 | D16 | 1.8 V | FM address bus |
| FM_A9 | E15 | 1.8 V | FM address bus |
| FM_A10 | E16 | 1.8 V | FM address bus |
| FM_A11 | H14 | 1.8 V | FM address bus |
| FM_A12 | D15 | 1.8 V | FM address bus |
| FM_A13 | F14 | 1.8 V | FM address bus |
| FM_A14 | C14 | 1.8 V | FM address bus |
| <i>continued...</i> | | | |

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|---------------------|
| FM_A15 | C15 | 1.8 V | FM address bus |
| FM_A16 | H3 | 1.8 V | FM address bus |
| FM_A17 | H2 | 1.8 V | FM address bus |
| FM_A18 | E13 | 1.8 V | FM address bus |
| FM_A19 | F13 | 1.8 V | FM address bus |
| FM_A20 | G13 | 1.8 V | FM address bus |
| FM_A21 | G12 | 1.8 V | FM address bus |
| FM_A22 | E12 | 1.8 V | FM address bus |
| FM_A23 | J13 | 1.8 V | FM address bus |
| FM_A24 | G5 | 1.8 V | FM address bus |
| FM_A25 | H13 | 1.8 V | FM address bus |
| FM_A26 | H4 | 1.8 V | FM address bus |
| FM_D0 | J15 | 1.8 V | FM data bus |
| FM_D1 | L16 | 1.8 V | FM data bus |
| FM_D2 | L14 | 1.8 V | FM data bus |
| FM_D3 | K14 | 1.8 V | FM data bus |
| FM_D4 | L13 | 1.8 V | FM data bus |
| FM_D5 | L15 | 1.8 V | FM data bus |
| FM_D6 | M15 | 1.8 V | FM data bus |
| FM_D7 | M16 | 1.8 V | FM data bus |
| FM_D8 | K16 | 1.8 V | FM data bus |
| FM_D9 | K15 | 1.8 V | FM data bus |
| FM_D10 | J14 | 1.8 V | FM data bus |
| FM_D11 | K13 | 1.8 V | FM data bus |
| FM_D12 | L12 | 1.8 V | FM data bus |
| FM_D13 | N16 | 1.8 V | FM data bus |
| FM_D14 | M13 | 1.8 V | FM data bus |
| FM_D15 | L11 | 1.8 V | FM data bus |
| FM_D16 | E4 | 1.8 V | FM data bus |
| FM_D17 | F6 | 1.8 V | FM data bus |
| FM_D18 | F4 | 1.8 V | FM data bus |
| FM_D19 | C2 | 1.8 V | FM data bus |
| FM_D20 | D1 | 1.8 V | FM data bus |
| FM_D21 | F1 | 1.8 V | FM data bus |
| FM_D22 | E3 | 1.8 V | FM data bus |
| FM_D23 | G2 | 1.8 V | FM data bus |
| | | | <i>continued...</i> |

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|--|
| FM_D24 | E5 | 1.8 V | FM data bus |
| FM_D25 | C3 | 1.8 V | FM data bus |
| FM_D26 | D3 | 1.8 V | FM data bus |
| FM_D27 | D2 | 1.8 V | FM data bus |
| FM_D28 | E1 | 1.8 V | FM data bus |
| FM_D29 | G3 | 1.8 V | FM data bus |
| FM_D30 | F3 | 1.8 V | FM data bus |
| FM_D31 | F2 | 1.8 V | FM data bus |
| FMCA_C2M_PG | R16 | 1.8 V | FMC port A power good output |
| FMCA_PRSENTN | G1 | 1.8 V | Green LED. Illuminates when the FMC port has a board or cable plugged-in. Driven by the add-in card. |
| FMCB_C2M_PG | L5 | 1.8 V | FMC port B power good output |
| FMCB_PRSENTN | E2 | 1.8 V | Green LED. Illuminates when the FMC port has a board or cable plugged-in. Driven by the add-in card. |
| FPGA_CONF_DONE | K1 | 1.8 V | FPGA configuration done LED |
| FPGA_CONFIG_D0 | R1 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D1 | T2 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D2 | N6 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D3 | N5 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D4 | N7 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D5 | N8 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D6 | M12 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D7 | T13 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D8 | T15 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D9 | R13 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D10 | P4 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D11 | R3 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D12 | T10 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D13 | P5 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D14 | R4 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D15 | R5 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D16 | M8 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D17 | M7 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D18 | T5 | 1.8 V | FPGA configuration data |
| <i>continued...</i> | | | |

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|--|
| FPGA_CONFIG_D19 | P9 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D20 | M6 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D21 | N9 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D22 | R8 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D23 | T8 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D24 | P7 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D25 | R7 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D26 | R9 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D27 | T9 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D28 | T7 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D29 | P8 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D30 | R6 | 1.8 V | FPGA configuration data |
| FPGA_CONFIG_D31 | P6 | 1.8 V | FPGA configuration data |
| FPGA_CVP_CONFDONE | M14 | 1.8 V | FPGA Configuration via Protocol (CvP) done |
| FPGA_DCLK | M9 | 1.8 V | FPGA configuration clock |
| FPGA_NCONFIG | E14 | 1.8 V | FPGA configuration active |
| FPGA_NSTATUS | J4 | 1.8 V | FPGA configuration ready |
| FPGA_PR_DONE | H12 | 1.8 V | FPGA partial reconfiguration done |
| FPGA_PR_ERROR | K12 | 1.8 V | FPGA partial reconfiguration error |
| FPGA_PR_READY | P12 | 1.8 V | FPGA partial reconfiguration ready |
| FPGA_PR_REQUEST | T4 | 1.8 V | FPGA partial reconfiguration request |
| M5_JTAG_TCK | P3 | 1.8 V | JTAG chain clock |
| M5_JTAG_TDI | L6 | 1.8 V | JTAG chain data in |
| M5_JTAG_TDO | M5 | 1.8 V | JTAG chain data out |
| M5_JTAG_TMS | N4 | 1.8 V | JTAG chain mode |
| MAX5_BEN0 | R10 | 1.8 V | MAX V Byte Enable 0 |
| MAX5_BEN1 | M10 | 1.8 V | MAX V Byte Enable 1 |
| MAX5_BEN2 | T12 | 1.8 V | MAX V Byte Enable 2 |
| MAX5_BEN3 | P10 | 1.8 V | MAX V Byte Enable 3 |
| MAX5_CLK | N11 | 1.8 V | MAX V Clock |
| MAX5_CSN | T11 | 1.8 V | MAX V chip select |
| MAX5_OEN | N10 | 1.8 V | MAX V output enable |
| MAX5_WEN | R11 | 1.8 V | MAX V Write enable |

continued...

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|--|
| MAX_CONF_DONE | D7 | 2.5 V | On-board USB-Blaster II configuration done LED |
| MAX_ERROR | C7 | 2.5 V | FPGA configuration error LED |
| MAX_LOAD | B6 | 2.5 V | FPGA configuration active LED |
| MAX_RESETN | J3 | 1.8 V | MAX V reset push button |
| MSEL0 | R12 | 1.8 V | FPGA MSEL0 setting |
| MSEL1 | P11 | 1.8 V | FPGA MSEL1 setting |
| MSEL2 | M11 | 1.8 V | FPGA MSEL2 setting |
| MV_CLK_50 | J12 | 1.8 V | MAX V 50 MHz clock |
| OVERTEMP | E11 | 2.5 V | Temperature monitor fan enable |
| OVERTEMPN | B16 | 2.5 V | Temperature monitor fan enable |
| PGM_CONFIG | A6 | 2.5 V | Load the flash memory image identified by the PGM LEDs |
| PGM_LED0 | D6 | 2.5 V | Flash memory PGM select indicator 0 |
| PGM_LED1 | C6 | 2.5 V | Flash memory PGM select indicator 1 |
| PGM_LED2 | B7 | 2.5 V | Flash memory PGM select indicator 2 |
| PGM_SEL | A7 | 2.5 V | Toggles the PGM_LED[2:0] LED sequence |
| SDI_MF0_BYPASS | P13 | 1.8 V | SDI Interface Mode Select 0 / Bypass control |
| SDI_MF1_AUTO_SLEEP | R14 | 1.8 V | SDI Interface Mode Select 1 / Auto Sleep Control |
| SDI_MF2_MUTE | N12 | 1.8 V | SDI Interface Mode Select 2 / Output Mute |
| SDI_TX_SD_HDN | N13 | 1.8 V | SDI Interface TX Signal Detect |
| SENSE_CS0N | D9 | 2.5 V | SPI Interface Chip Select |
| SENSE_SCK | B9 | 2.5 V | SPI Interface Clock |
| SENSE_SDI | B3 | 2.5 V | SPI Interface Serial Data In |
| SENSE_SDO | C9 | 2.5 V | SPI Interface Serial Data Out |
| SENSE_SMB_CLK | A15 | 2.5 V | I ₂ C Interface Clock |
| SENSE_SMB_DATA | B13 | 2.5 V | I ₂ C Interface Data |
| SI516_FS | C5 | 2.5 V | Silicon Labs SI516 Clock Device Frequency Select |
| continued... | | | |

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|---|
| SI570_EN | A10 | 2.5 V | SI570 programmable clock enable |
| TSENSE_ALERTN | B14 | 2.5 V | MAX1619 device Temperature Sense Alert Signal |
| USB_CFG0 | M4 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG1 | M3 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG2 | K2 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG3 | K5 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG4 | L1 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG5 | L2 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG6 | K3 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG7 | M2 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG8 | L4 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG9 | L3 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG10 | N1 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG11 | N2 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG12 | M1 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG13 | N3 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_CFG14 | P2 | 1.8 V | On-board USB-Blaster II interface (reserved for future use) |
| USB_M5_CLK | H5 | 1.8 V | On-board USB-Blaster II interface clock |

continued...

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|-------------------------|
| ED8101_ALERT | B8 | 2.5 V | ED8101 Alert signal |
| ED8101_SCL | A8 | 2.5 V | ED8101 I2C clock signal |
| ED8101_SDA | A9 | 2.5 V | ED8101 I2C data signal |

6.3. FPGA Configuration

6.3.1. Configuring the FPGA Using Programmer

You can use the Quartus Programmer to configure the FPGA with your SRAM Object File (.sof).

Ensure the following:

- The Quartus Programmer and the USB-Blaster II driver are installed on the host computer.
 - The micro-USB cable is connected to the FPGA development board.
 - Power to the board is on, and no other applications that use the JTAG chain are running.
1. Start the Quartus Programmer.
 2. Click **Auto Detect** to display the devices in the JTAG chain.
 3. Click **Change File** and select the path to the desired .sof.
 4. Turn on the **Program/Configure** option for the added file.
 5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Using the Quartus Programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

6.4. Status Elements

The Arria 10 GX FPGA development board includes status LEDs.

Table 17. Board-Specific LEDs

| Board Reference | Schematic Signal Name | I/O Standard |
|---------------------|-----------------------|--------------|
| D16 | MAX_ERROR | 2.5 V |
| D15 | MAX_LOAD | 2.5 V |
| D17 | MAX_CONF_DONE | 2.5 V |
| D1 | FMCA_TX_LED | 1.8 V |
| D2 | FMCA_RX_LED | 1.8 V |
| D12 | PGM_LED0 | 2.5 V |
| D13 | PGM_LED1 | 2.5 V |
| D14 | PGM_LED2 | 2.5 V |
| <i>continued...</i> | | |

| Board Reference | Schematic Signal Name | I/O Standard |
|-----------------|-----------------------|--------------|
| D11 | FMCA_PRSENTn | 1.8 V |
| D18 | FMCB_TX_LED | 1.8 V |
| D20 | FMCB_RX_LED | 1.8 V |
| D21 | FMCB_PRSENTn | 1.8 V |
| D34 | PCIE_LED_X1 | 1.8 V |
| D35 | PCIE_LED_X4 | 1.8 V |
| D36 | PCIE_LED_X8 | 1.8 V |
| D37 | PCIE_LED_G2 | 1.8 V |
| D38 | PCIE_LED_G3 | 1.8 V |

6.5. User Input/Output

6.5.1. User-Defined Push Buttons

The Arria 10 GX FPGA development board includes user-defined push buttons. When you press and hold down the button, the device pin is set to logic 0; when you release the button, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 18. User-Defined Push Button Schematic Signal Names and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|--------------|
| S1 | USER_PB2 | U11 | 1.8 V |
| S2 | USER_PB1 | U12 | 1.8 V |
| S3 | USER_PB0 | T12 | 1.8 V |
| S4 | CPU_RESETh | BD27 | 1.8 V |
| S5 | PGM_SEL | — | 2.5 V |
| S6 | PGM_CONFIG | — | 2.5 V |
| S7 | MAX_RESETh | — | 2.5 V |

6.5.2. User-Defined DIP Switch

The Arria 10 GX FPGA development board includes a set of eight-pin DIP switch. There are no board-specific functions for these switches. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected.

Table 19. User-Defined DIP Switch Schematic Signal Names and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|--------------|
| 1 | USER_DIPSW0 | A24 | 1.8-V |
| 2 | USER_DIPSW1 | B23 | 1.8-V |
| 3 | USER_DIPSW2 | A23 | 1.8-V |
| 4 | USER_DIPSW3 | B22 | 1.8-V |
| 5 | USER_DIPSW4 | A22 | 1.8-V |
| 6 | USER_DIPSW5 | B21 | 1.8-V |
| 7 | USER_DIPSW6 | C21 | 1.8-V |
| 8 | USER_DIPSW7 | A20 | 1.8-V |

6.5.3. User-Defined LEDs

The Arria 10 GX FPGA development board includes a set of eight pairs user-defined LEDs. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There are no board-specific functions for these LEDs.

Table 20. User-Defined LEDs Schematic Signal Names and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|--------------|
| D10 | USER_LED_G0 | L28 | 1.8 V |
| D9 | USER_LED_G1 | K26 | 1.8 V |
| D8 | USER_LED_G2 | K25 | 1.8 V |
| D7 | USER_LED_G3 | L25 | 1.8 V |
| D6 | USER_LED_G4 | J24 | 1.8 V |
| D5 | USER_LED_G5 | A19 | 1.8 V |
| D4 | USER_LED_G6 | C18 | 1.8 V |
| D3 | USER_LED_G7 | D18 | 1.8 V |
| D10 | USER_LED_R0 | L27 | 1.8 V |
| D9 | USER_LED_R1 | J26 | 1.8 V |
| D8 | USER_LED_R2 | K24 | 1.8 V |
| D7 | USER_LED_R3 | L23 | 1.8 V |
| D6 | USER_LED_R4 | B20 | 1.8 V |
| D5 | USER_LED_R5 | C19 | 1.8 V |
| D4 | USER_LED_R6 | D19 | 1.8 V |
| D3 | USER_LED_R7 | M23 | 1.8 V |

6.5.4. Character LCD

The Arria 10 GX FPGA development board includes a single 10-pin 0.1" pitch single-row header that interfaces to a 16 character × 2 line Lumex LCD display. The LCD has a 10-pin receptacle that mounts directly to the board's 10-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

Table 21. Character LCD Schematic Signal Names and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------|-----------------------------------|-----------------|--------------|--|
| 5 | SPI_SS_DISP / DISP_SPISS | BA35 | 1.8 V | SPI slave select (only used in SPI mode) |
| 7 | I2C_SCL_DISP / DISP_I2C_SCL | AW33 | 1.8 V | I ² C LCD serial clock |
| 8 | I2C_SDA_DISP / DISP_I2C_SDA | AY34 | 1.8 V | I ² C LCD serial data |

6.5.5. DisplayPort

The Arria 10 GX FPGA development board includes a DisplayPort connector.

Table 22. DisplayPort Schematic Signal Names and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------|-----------------------|-----------------|-----------------------------|------------------------------|
| 13 | DP_3P3V_CONFIG 1 | AK31 | 1.8 V | — |
| 14 | DP_3P3V_CONFIG 2 | AK32 | 1.8 V | — |
| 18 | DP_3P3V_HOT_PLUG | AM30 | 1.8 V | Hot plug detect |
| 17 | DP_AUX_CN | AM35 | LVDS | Auxiliary channel (negative) |
| 15 | DP_AUX_CP | AN34 | LVDS | Auxiliary channel (positive) |
| 3 | DP_ML_LANE_CN 0 | AP43 | High Speed Differential I/O | Lane 0 (negative) |
| 6 | DP_ML_LANE_CN 1 | AM43 | High Speed Differential I/O | Lane 1 (negative) |
| 9 | DP_ML_LANE_CN 2 | AH43 | High Speed Differential I/O | Lane 2 (negative) |
| 12 | DP_ML_LANE_CN 3 | AF43 | High Speed Differential I/O | Lane 3 (negative) |
| 1 | DP_ML_LANE_CP0 | AP44 | High Speed Differential I/O | Lane 0 (positive) |
| 4 | DP_ML_LANE_CP1 | AM44 | High Speed Differential I/O | Lane 1 (positive) |
| 7 | DP_ML_LANE_CP2 | AH44 | High Speed Differential I/O | Lane 2 (positive) |
| 10 | DP_ML_LANE_CP3 | AF44 | High Speed Differential I/O | Lane 3 (positive) |
| 19 | DP_RTN | AL33 | High Speed Differential I/O | Return for power |

6.5.6. SDI Video Input/Output Ports

The Arria 10 GX FPGA development board includes a SDI video port, which consists of a M23428G-33 cable driver and a M23544G-14 cable equalizer. The PHY devices from Macom interface to single-ended SMB connectors.

The cable driver supports operation from 125 Mbps to 11.88 Gbps. Control signals are allowed for SD and HD modes selections, as well as device enable. The device can be clocked by the 148.5 MHz voltage-controlled crystal oscillator (VCXO) and matched to incoming signals within 50 ppm using the UP and DN voltage control lines to the VCXO.

Table 23. SDI Video Output Standards for the SD and HD Input

| SD_HD Input | Supported Output Standards | Rise Time |
|-------------|----------------------------|-----------|
| 0 | SMPTE 424M, SMPTE 292M | Faster |
| 1 | SMPTE 259M | Slower |

Table 24. SDI Video Output Interface Pin Assignments, Schematic Signal Names, and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|-----------------------------|
| 14 | SDI_AVDD | — | — |
| 2 | SDI_AVDD | — | — |
| 7 | SDI_AVDD | — | — |
| 9 | SDI_SD_HDN | AW34 | 1.8 V |
| 5 | SDI_TX_RSET | — | — |
| 1 | SDI_TXCAP_N | D43 | High Speed Differential I/O |
| 16 | SDI_TXCAP_P | D44 | High Speed Differential I/O |
| 10 | SDI_TXDRV_N | — | — |
| 11 | SDI_TXDRV_P | — | — |

Table 25. SDI Cable Equalizer Lengths

The cable equalizer supports operation at 270 Mbit SD, 1.5 Gbit HD, and 3.0, 6.0, and 11.88 Gbit dual-link HD modes. Control signals are allowed for bypassing or disabling the device, as well as a carrier detect or auto-mute signal interface.

| Cable Type | Data Rate (Mbps) | Maximum Cable Length (m) |
|--------------|------------------|--------------------------|
| Belden 1694A | 270 | 400 |
| Belden 1694A | 1485 | 140 |
| Belden 1694A | 2970 | 120 |

Table 26. SDI Video Input Interface Pin Assignments, Schematic Signal Names, and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------|-----------------------|-----------------|--------------|
| 9 | AGCN | — | — |
| 8 | AGXP | — | — |
| 10 | MF0_BYPASS | AW32 | 1.8 V |
| <i>continued...</i> | | | |

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|-----------------------------|
| 19 | MF1_AUTO_SLEEP | AY32 | 1.8 V |
| 21 | MF2_MUTE | AY35 | 1.8 V |
| 22 | MF3_XSD | — | — |
| 6 | MODE_SEL | — | — |
| 11 | MUTEREF | — | — |
| 4 | SDI_EQIN_N1 | — | — |
| 3 | SDI_EQIN_P1 | — | — |
| 14 | SDO_N / SDI_RX_N | H39 | High Speed Differential I/O |
| 15 | SDO_P / SDI_RX_P | H40 | High Speed Differential I/O |

6.6. Clock Circuitry

6.6.1. On-Board Oscillators

Figure 32. Arria 10 GX FPGA Kit Board Clock Inputs and Default Frequencies

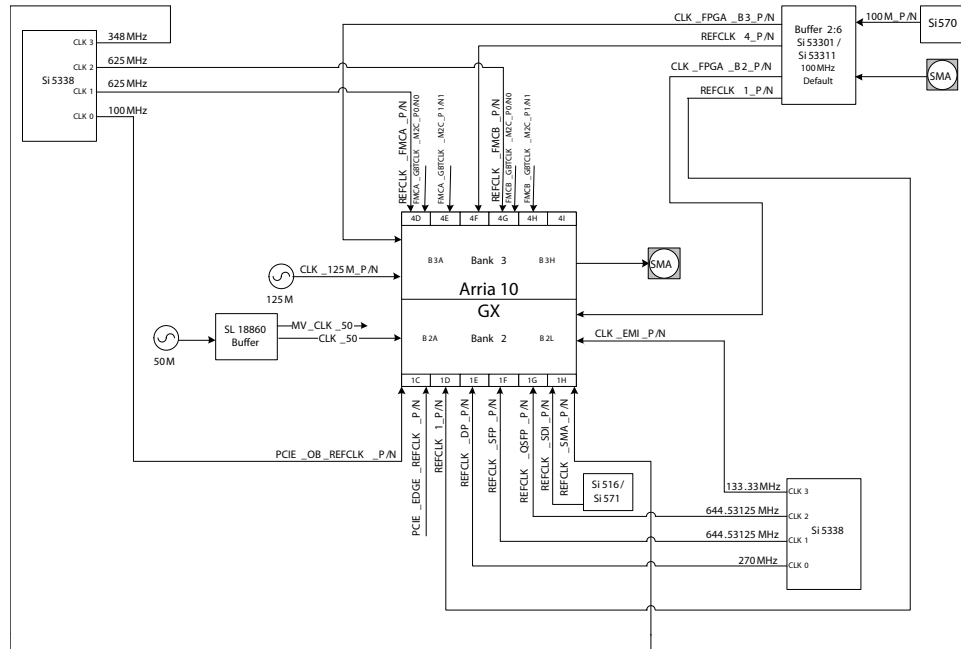


Table 27. On-Board Oscillators

| Source | Schematic Signal Name | Frequency | I/O Standard | Arria 10 FPGA Pin Number | Application |
|--------|-----------------------|----------------|--------------|--------------------------|--------------------------------------|
| U14 | REFCLK_SMA_P | 302.083333 MHz | 1.8 V LVDS | N37 | Transceiver reference clocks Bank-1H |
| | REFCLK_SMA_N | | 1.8 V LVDS | N38 | |
| | REFCLK_FMCB_P | 625 MHz | 1.8 V LVDS | AA8 | FMC B reference clocks |
| | REFCLK_FMCB_N | | 1.8 V LVDS | AA7 | |
| | REFCLK_FMCA_P | 625 MHz | 1.8 V LVDS | AN8 | FMC A reference clocks |
| | REFCLK_FMCA_N | | 1.8 V LVDS | AN7 | |
| | PCIE_OB_REFCLK_P | 100 MHz | 1.8 V LVDS | AN37 | PCIE reference clocks |
| | PCIE_OB_REFCLK_N | | 1.8 V LVDS | AN38 | |
| U26 | CLK_EMI_P | 133.33 MHz | 1.8 V LVDS | F34 | EMI reference clocks |
| | CLK_EMI_N | | 1.8 V LVDS | F35 | |
| | REFCLK_QSFP_P | 644.53125 MHz | 1.8 V LVDS | R37 | QSFP reference clocks |

continued...

| Source | Schematic Signal Name | Frequency | I/O Standard | Arria 10 FPGA Pin Number | Application |
|--------|-----------------------|---------------|--------------|--------------------------|--|
| X1 | REFCLK_QSFP_N | | 1.8 V LVDS | R38 | SFP reference clocks |
| | REFCLK_SFP_P | 644.53125 MHz | 1.8 V LVDS | AA37 | |
| | REFCLK_SFP_N | | 1.8 V LVDS | AA38 | Display port (DP) reference clocks |
| | REFCLK_DP_P | 270 MHz | 1.8 V LVDS | AC37 | |
| | REFCLK_DP_N | | 1.8 V LVDS | AC38 | |
| | REFCLK_SDI_P | 148.35 MHz | 1.8 V LVDS | L37 | |
| | REFCLK_SDI_N | | 1.8 V LVDS | L38 | |
| X2 | CLK_125_P | 125 MHz | 1.8 V LVDS | BD24 | 125 MHz reference clocks for Arria 10 FPGA |
| | CLK_125_N | | 1.8 V LVDS | BC24 | |
| X3 | 100M_OSC_P | 100 MHz | LVDS | AR36, F23, AG37, AC8 | Programmable Oscillator default 100MHz |
| | 100M_OSC_N | | LVDS | AR37, G23, AG38, AC7 | |
| U53 | MV_CLK_50 | 50 MHz | 1.8 V | - | MAX V System Controller clock |
| | CLK_50 | | 1.8 V | AU33 | Arria 10 FPGA reference clock |

6.6.2. Off-Board Clock I/O

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 28. Off-Board Clock Inputs

| Source | Schematic Signal Name | I/O Standard | Arria 10 FPGA Pin Number | Description |
|--------|-----------------------|--------------|--------------------------|-----------------|
| J6 | CLKIN_SMA | 2.5 V | - | SMA clock input |

Table 29. Off-Board Clock Outputs

| Source | Schematic Signal Name | I/O Standard | Arria 10 FPGA Pin Number | Description |
|--------|-----------------------|--------------|--------------------------|---------------------|
| J7 | SMA_CLK_OUT | 1.8 V | E24 | SMA clock output |
| J16 | SMA_TX_P | 1.8 V | C42 | SMA transfer clocks |
| J15 | SMA_TX_N | 1.8 V | C41 | |

6.7. Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Arria 10 GX FPGA device.

6.7.1. PCI Express

The Arria 10 GX FPGA development board is designed to fit entirely into a PC motherboard with a ×8 PCI Express slot that can accommodate a full height long form factor add-in card. This interface uses the Arria 10 GX FPGA's PCI Express hard IP block, saving logic resources for the user logic application. The PCI express edge connector has a presence detect feature to allow the motherboard to determine if a card is installed.

The PCI Express interface supports auto-negotiating channel width from ×1 to ×4 to ×8 by using Altera's PCIe MegaCore IP. You can also configure this board to a ×1, ×4, or ×8 interface through a DIP switch that connects the PRSNTn pins for each bus width.

The PCI Express edge connector has a connection speed of 2.5 Gbps/lane for a maximum of 20 Gbps full-duplex (Gen1), 5.0 Gbps/lane for a maximum of 40 Gbps full-duplex (Gen2), or 8.0 Gbps/lane for a maximum of 64 Gbps full-duplex (Gen3).

The power for the board can be sourced entirely from the PC host when installed into a PC motherboard with the PC's 2x4 ATX auxiliary power connected to the 12V ATX input (J4) of the Arria 10 development board. Although the board can also be powered by a laptop power supply for use on a lab bench, Altera recommends that you do not power up from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The PCIE_REFCLK_P signal is a 100 MHz differential input that is driven from the PC motherboard on to this board through the edge connector. This signal connects directly to a Arria 10 GX FPGA REFCLK input pin pair using DC coupling. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL). The JTAG and SMB are optional signals in the PCI Express specification. Therefore, the JTAG signal loopback from PCI Express TDI to PCI Express TDO and are not used on this board. The SMB signals are wired to the Arria 10 GX FPGA but are not required for normal operation.

Table 30. PCI Express Pin Assignments, Schematic Signal Names, and Functions

| Receive bus | Receive bus | FPGA Pin Number | I/O Standard | Description |
|---------------------|------------------------|-----------------|--------------|-----------------------------|
| A11 | PCIE_EDGE_PERS TN | BC30 | 1.8 V | Reset |
| A14 | PCIE_EDGE_REFC LK_N | AL38 | LVDS | Motherboard reference clock |
| A13 | PCIE_EDGE_REFC LK_P | AL37 | LVDS | Motherboard reference clock |
| B5 | PCIE_EDGE_SMBC LK | BD29 | 1.8 V | SMB clock |
| <i>continued...</i> | | | | |

| Receive bus | Receive bus | FPGA Pin Number | I/O Standard | Description |
|---------------------|-------------------|-----------------|-----------------------------|----------------------|
| B6 | PCIE_EDGE_SMB DAT | AU37 | 1.8 V | SMB data |
| A1 | PCIE_PRSENT1N | — | — | Link with DIP switch |
| B17 | PCIE_PRSENT2N_X 1 | — | — | Link with DIP switch |
| B31 | PCIE_PRSENT2N_X 4 | — | — | Link with DIP switch |
| B48 | PCIE_PRSENT2N_X 8 | — | — | Link with DIP switch |
| B15 | PCIE_RX_N0 | AT39 | High Speed Differential I/O | Receive bus |
| B20 | PCIE_RX_N1 | AP39 | High Speed Differential I/O | Receive bus |
| B24 | PCIE_RX_N2 | AN41 | High Speed Differential I/O | Receive bus |
| B28 | PCIE_RX_N3 | AM39 | High Speed Differential I/O | Receive bus |
| B34 | PCIE_RX_N4 | AL41 | High Speed Differential I/O | Receive bus |
| B38 | PCIE_RX_N5 | AK39 | High Speed Differential I/O | Receive bus |
| B42 | PCIE_RX_N6 | AJ41 | High Speed Differential I/O | Receive bus |
| B46 | PCIE_RX_N7 | AH39 | High Speed Differential I/O | Receive bus |
| B14 | PCIE_RX_P0 | AT40 | High Speed Differential I/O | Receive bus |
| B19 | PCIE_RX_P1 | AP40 | High Speed Differential I/O | Receive bus |
| B23 | PCIE_RX_P2 | AN42 | High Speed Differential I/O | Receive bus |
| B27 | PCIE_RX_P3 | AM40 | High Speed Differential I/O | Receive bus |
| B33 | PCIE_RX_P4 | AL42 | High Speed Differential I/O | Receive bus |
| B37 | PCIE_RX_P5 | AK40 | High Speed Differential I/O | Receive bus |
| B41 | PCIE_RX_P6 | AJ42 | High Speed Differential I/O | Receive bus |
| B45 | PCIE_RX_P7 | AH40 | High Speed Differential I/O | Receive bus |
| A17 | PCIE_TX_CN0 | BB43 | High Speed Differential I/O | Transmit bus |
| A22 | PCIE_TX_CN1 | BA41 | High Speed Differential I/O | Transmit bus |
| A26 | PCIE_TX_CN2 | AY43 | High Speed Differential I/O | Transmit bus |
| <i>continued...</i> | | | | |

| Receive bus | Receive bus | FPGA Pin Number | I/O Standard | Description |
|-------------|--------------|-----------------|-----------------------------|--------------|
| A30 | PCIE_TX_CN3 | AW41 | High Speed Differential I/O | Transmit bus |
| A36 | PCIE_TX_CN4 | AV43 | High Speed Differential I/O | Transmit bus |
| A40 | PCIE_TX_CN5 | AU41 | High Speed Differential I/O | Transmit bus |
| A44 | PCIE_TX_CN6 | AT43 | High Speed Differential I/O | Transmit bus |
| A48 | PCIE_TX_CN7 | AR41 | High Speed Differential I/O | Transmit bus |
| A16 | PCIE_TX_CP0 | BB44 | High Speed Differential I/O | Transmit bus |
| A21 | PCIE_TX_CP1 | BA42 | High Speed Differential I/O | Transmit bus |
| A25 | PCIE_TX_CP2 | AY44 | High Speed Differential I/O | Transmit bus |
| A29 | PCIE_TX_CP3 | AW42 | High Speed Differential I/O | Transmit bus |
| A35 | PCIE_TX_CP4 | AV44 | High Speed Differential I/O | Transmit bus |
| A39 | PCIE_TX_CP5 | AU42 | High Speed Differential I/O | Transmit bus |
| A43 | PCIE_TX_CP6 | AT44 | High Speed Differential I/O | Transmit bus |
| A47 | PCIE_TX_CP7 | AR42 | High Speed Differential I/O | Transmit bus |
| B11 | PCIE_WAKEN_R | AY29 | 1.8 V | Wake signal |

6.7.2. 10/100/1000 Ethernet PHY

The Arria 10 GX FPGA development board supports 10/100/1000 base-T Ethernet using an external Marvell 88E1111 PHY and Altera Triple-Speed Ethernet MegaCore MAC function. The PHY-to-MAC interface employs SGMII using the Arria 10 GX FPGA LVDS pins in Soft-CDR mode at 1.25 Gbps transmit and receive. In 10-Mb or 100-Mb mode, the SGMII interface still runs at 1.25 GHz but the packet data is repeated 10 or 100 times. The MAC function must be provided in the FPGA for typical networking applications.

The Marvell 88E1111 PHY uses 2.5-V and 1.0-V power rails and requires a 25 MHz reference clock driven from a dedicated oscillator. The PHY interfaces to a HALO HFJ11-1G02E model RJ45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 33. SGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

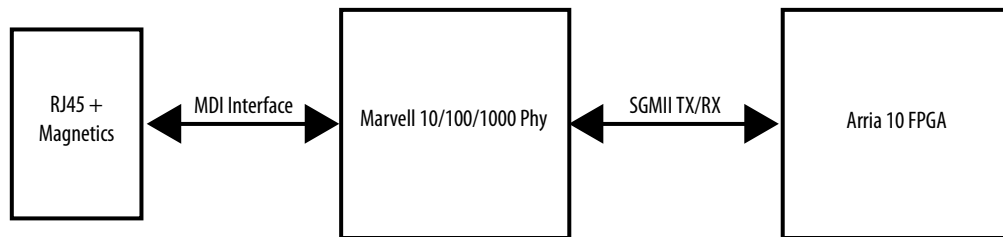


Table 31. Ethernet PHY Pin Assignments, Signal Names and Functions

| Board Reference (U15) | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------------|-----------------------|-----------------|--------------|---------------------------|
| 23 | ENET_2P5V_INTN | AG13 | 1.8 V | Management bus interrupt |
| 25 | ENET_2P5V_MDC | AF13 | 1.8 V | Management bus data clock |
| 24 | ENET_2P5V_MDIO | AL18 | 1.8 V | Management bus data |
| 28 | ENET_2P5V_RESE TN | AW23 | 1.8 V | Device reset |
| 59 | ENET_LED_LINK1 0 | — | 2.5 V | 10-Mb link LED |
| 76 | ENET_LED_LINK1 0 | — | 2.5 V | 10-Mb link LED |
| 74 | ENET_LED_LINK1 00 | — | 2.5 V | 100-Mb link LED |
| 60 | ENET_LED_LINK1 000 | — | 2.5 V | 1000-Mb link LED |
| 73 | ENET_LED_LINK1 000 | — | 2.5 V | 1000-Mb link LED |
| 58 | ENET_LED_RX | — | 2.5 V | RX data active LED |
| 69 | ENET_LED_RX | — | 2.5 V | RX data active LED |
| 68 | ENET_LED_TX | — | 2.5 V | TX data active LED |
| 30 | ENET_RSET | AW23 | 1.8 V | Device reset |
| 75 | ENET_RX_N | AW24 | LVDS | SGMII receive channel |

continued...

| Board Reference (U15) | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------------|-----------------------|-----------------|--------------|-----------------------------|
| 77 | ENET_RX_P | AV24 | 2.5 V | SGMII receive channel |
| 81 | ENET_TX_N | BD23 | | SGMII transmit channel |
| 82 | ENET_TX_P | BC23 | | SGMII transmit channel |
| 55 | ENET_XTAL_25MHZ | — | | 25-MHz RGMII transmit clock |
| 31 | MDI_N0 | — | | Media dependent interface |
| 34 | MDI_N1 | — | | |
| 41 | MDI_N2 | — | | |
| 43 | MDI_N3 | — | | |
| 29 | MDI_P0 | — | | |
| 33 | MDI_P1 | — | | |
| 39 | MDI_P2 | — | | |
| 42 | MDI_P3 | — | | |

6.7.3. HiLo External Memory Interface

This section describes the Arria 10 GX FPGA development board's external memory interface support and also their signal names, types, and connectivity relative to the Arria 10 GX FPGA.

The HiLo connector supports plugins the following memory interfaces:

- DDR3 x72 (included in the kit)
- DDR4 x72 (included in the kit)
- RLDRAM3 x36 (included in the kit)
- QDR IV x36 (not included. Contact your local Altera sales representative for ordering and availability)

Table 32. HiLo EMI Pin Assignments, Schematic Signal Names

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|--------------|
| F1 | MEM_ADDR_CMD0 | M32 | 1.5 V |
| H1 | MEM_ADDR_CMD1 | L32 | 1.5 V |
| F2 | MEM_ADDR_CMD2 | N34 | 1.5 V |
| G2 | MEM_ADDR_CMD3 | M35 | 1.5 V |
| H2 | MEM_ADDR_CMD4 | L34 | 1.5 V |
| J2 | MEM_ADDR_CMD5 | K34 | 1.5 V |
| K2 | MEM_ADDR_CMD6 | M33 | 1.5 V |
| G3 | MEM_ADDR_CMD7 | L33 | 1.5V |
| J3 | MEM_ADDR_CMD8 | J33 | 1.5 V |
| L3 | MEM_ADDR_CMD9 | J32 | 1.5 V |
| E4 | MEM_ADDR_CMD10 | H31 | 1.5 V |
| F4 | MEM_ADDR_CMD11 | J31 | 1.5 V |
| G4 | MEM_ADDR_CMD12 | H34 | 1.5 V |
| H4 | MEM_ADDR_CMD13 | H33 | 1.5 V |
| J4 | MEM_ADDR_CMD14 | G32 | 1.5 V |
| K4 | MEM_ADDR_CMD15 | E32 | 1.5 V |
| M1 | MEM_ADDR_CMD16 | F33 | 1.5 V |
| M2 | MEM_ADDR_CMD17 | G35 | 1.5 V |
| N2 | MEM_ADDR_CMD18 | H35 | 1.5 V |
| L4 | MEM_ADDR_CMD19 | G33 | 1.5 V |
| P5 | MEM_ADDR_CMD20 | U33 | 1.5 V |
| M5 | MEM_ADDR_CMD21 | T33 | 1.5 V |
| P1 | MEM_ADDR_CMD22 | R34 | 1.5 V |
| R4 | MEM_ADDR_CMD23 | P34 | 1.5 V |
| M4 | MEM_ADDR_CMD24 | N33 | 1.5 V |

continued...

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------|-----------------------|-----------------|--------------|
| R3 | MEM_ADDR_CMD25 | P33 | 1.5 V |
| L2 | MEM_ADDR_CMD26 | F32 | 1.5 V |
| K1 | MEM_ADDR_CMD27 | T35 | 1.5 V |
| P2 | MEM_ADDR_CMD28 | T34 | 1.5 V |
| N4 | MEM_ADDR_CMD29 | E35 | 1.5 V |
| P4 | MEM_ADDR_CMD30 | U32 | 1.5 V |
| N3 | MEM_ADDR_CMD31 | T32 | 1.5 V |
| V2 | MEM_CLK_N | R31 | 1.5 V |
| V1 | MEM_CLK_P | R30 | 1.5 V |
| B10 | MEM_DMA0 | E26 | 1.5 V |
| C4 | MEM_DMA1 | G27 | 1.5 V |
| B17 | MEM_DMA2 | A29 | 1.5 V |
| F17 | MEM_DMA3 | F30 | 1.5 V |
| M16 | MEM_DMB0 | AB32 | 1.5 V |
| U16 | MEM_DMB1 | AG31 | 1.5 V |
| U11 | MEM_DMB2 | Y35 | 1.5 V |
| U6 | MEM_DMB3 | AC34 | 1.5 V |
| R6 | MEM_DQ_ADDR_CMD0 | A32 | 1.5 V |
| T1 | MEM_DQ_ADDR_CMD1 | A33 | 1.5 V |
| R2 | MEM_DQ_ADDR_CMD2 | B32 | 1.5 V |
| T2 | MEM_DQ_ADDR_CMD3 | D32 | 1.5 V |
| U2 | MEM_DQ_ADDR_CMD4 | C33 | 1.5 V |
| U3 | MEM_DQ_ADDR_CMD5 | B33 | 1.5 V |
| T4 | MEM_DQ_ADDR_CMD6 | D34 | 1.5 V |
| U4 | MEM_DQ_ADDR_CMD7 | C35 | 1.5 V |
| T5 | MEM_DQ_ADDR_CMD8 | E34 | 1.5 V |
| A4 | MEM_DQA0 | B28 | 1.5 V |
| B4 | MEM_DQA1 | A28 | 1.5 V |
| B5 | MEM_DQA2 | A27 | 1.5 V |
| B6 | MEM_DQA3 | B27 | 1.5 V |
| A8 | MEM_DQA4 | D27 | 1.5 V |
| B8 | MEM_DQA5 | E27 | 1.5 V |
| B9 | MEM_DQA6 | D26 | 1.5 V |
| A10 | MEM_DQA7 | D28 | 1.5 V |
| B1 | MEM_DQA8 | G25 | 1.5 V |
| B2 | MEM_DQA9 | H25 | 1.5 V |
| <i>continued...</i> | | | |

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|---------------------|
| C2 | MEM_DQA10 | G26 | 1.5 V |
| C3 | MEM_DQA11 | H26 | 1.5 V |
| E3 | MEM_DQA12 | G28 | 1.5 V |
| D4 | MEM_DQA13 | F27 | 1.5 V |
| D1 | MEM_DQA14 | K27 | 1.5 V |
| D2 | MEM_DQA15 | F28 | 1.5 V |
| A12 | MEM_DQA16 | D31 | 1.5 V |
| B12 | MEM_DQA17 | E31 | 1.5 V |
| B13 | MEM_DQA18 | B31 | 1.5 V |
| B14 | MEM_DQA19 | C31 | 1.5 V |
| C15 | MEM_DQA20 | A30 | 1.5 V |
| A16 | MEM_DQA21 | E30 | 1.5 V |
| B16 | MEM_DQA22 | B30 | 1.5 V |
| A18 | MEM_DQA23 | D29 | 1.5 V |
| C16 | MEM_DQA24 | K30 | 1.5 V |
| D16 | MEM_DQA25 | H30 | 1.5 V |
| E16 | MEM_DQA26 | G30 | 1.5 V |
| F16 | MEM_DQA27 | K31 | 1.5 V |
| D17 | MEM_DQA28 | H29 | 1.5 V |
| C18 | MEM_DQA29 | K29 | 1.5 V |
| D18 | MEM_DQA30 | J29 | 1.5 V |
| E18 | MEM_DQA31 | F29 | 1.5 V |
| E2 | MEM_DQA32 | J28 | 1.5 V |
| G16 | MEM_DQA33 | G31 | 1.5 V |
| H16 | MEM_DQB0 | AC31 | 1.5 V |
| J16 | MEM_DQB1 | AB31 | 1.5 V |
| K16 | MEM_DQB2 | W31 | 1.5 V |
| L16 | MEM_DQB3 | Y31 | 1.5 V |
| H17 | MEM_DQB4 | AD31 | 1.5 V |
| K17 | MEM_DQB5 | AD32 | 1.5 V |
| K18 | MEM_DQB6 | AD33 | 1.5 V |
| L18 | MEM_DQB7 | AA30 | 1.5 V |
| M17 | MEM_DQB8 | AE31 | 1.5 V |
| N18 | MEM_DQB9 | AE32 | 1.5 V |
| P17 | MEM_DQB10 | AE30 | 1.5 V |
| P18 | MEM_DQB11 | AF30 | 1.5 V |
| | | | <i>continued...</i> |

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------|-----------------------|-----------------|--------------|
| R18 | MEM_DQB12 | AG33 | 1.5 V |
| T16 | MEM_DQB13 | AG32 | 1.5 V |
| T17 | MEM_DQB14 | AH33 | 1.5 V |
| T18 | MEM_DQB15 | AH31 | 1.5 V |
| U15 | MEM_DQB16 | U31 | 1.5 V |
| T14 | MEM_DQB17 | W33 | 1.5 V |
| U14 | MEM_DQB18 | W32 | 1.5 V |
| V14 | MEM_DQB19 | V31 | 1.5 V |
| T13 | MEM_DQB20 | Y34 | 1.5 V |
| T12 | MEM_DQB21 | W35 | 1.5 V |
| U12 | MEM_DQB22 | W34 | 1.5 V |
| V12 | MEM_DQB23 | V34 | 1.5 V |
| T10 | MEM_DQB24 | AH35 | 1.5 V |
| U10 | MEM_DQB25 | AJ34 | 1.5 V |
| V10 | MEM_DQB26 | AJ33 | 1.5 V |
| T9 | MEM_DQB27 | AH34 | 1.5 V |
| T8 | MEM_DQB28 | AD35 | 1.5 V |
| U8 | MEM_DQB29 | AE34 | 1.5 V |
| U7 | MEM_DQB30 | AC33 | 1.5 V |
| V6 | MEM_DQB31 | AD34 | 1.5 V |
| R16 | MEM_DQB32 | AF32 | 1.5 V |
| T6 | MEM_DQB33 | AB33 | 1.5 V |
| V5 | MEM_DQS_ADDR_CMD_N | C34 | 1.5 V |
| V4 | MEM_DQS_ADDR_CMD_P | D33 | 1.5 V |
| A7 | MEM_DQSA_N0 | C26 | 1.5 V |
| A3 | MEM_DQSA_N1 | J27 | 1.5 V |
| A15 | MEM_DQSA_N2 | C29 | 1.5 V |
| G18 | MEM_DQSA_N3 | L29 | 1.5 V |
| A6 | MEM_DQSA_P0 | B26 | 1.5 V |
| A2 | MEM_DQSA_P1 | H28 | 1.5 V |
| A14 | MEM_DQSA_P2 | C30 | 1.5 V |
| F18 | MEM_DQSA_P3 | L30 | 1.5 V |
| J18 | MEM_DQSB_N0 | AA32 | 1.5 V |
| V18 | MEM_DQSB_N1 | AJ31 | 1.5 V |
| V17 | MEM_DQSB_N2 | AA33 | 1.5 V |
| V9 | MEM_DQSB_N3 | AF34 | 1.5 V |
| <i>continued...</i> | | | |

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|--------------|
| H18 | MEM_DQSB_P0 | Y32 | 1.5 V |
| U18 | MEM_DQSB_P1 | AJ32 | 1.5 V |
| V16 | MEM_DQSB_P2 | AA34 | 1.5 V |
| V8 | MEM_DQSB_P3 | AF33 | 1.5 V |
| A11 | MEM_QKA_P0 | C28 | 1.5 V |
| B18 | MEM_QKA_P1 | E29 | 1.5 V |
| M18 | MEM_QKB_P0 | Y30 | 1.5 V |
| V13 | MEM_QKB_P1 | V33 | 1.5 V |
| H14 | MEM_VREF | AB30 | — |
| J13 | MEM_VREF | K32 | — |
| K14 | MEM_VREF | R32 | — |

Related Information

[External Memory Interfaces in Arria 10 Devices](#)

6.7.4. FMC

The Arria 10 GX FPGA development board includes a high pin count (HPC) FPGA mezzanine card (FMC) connector that functions with a quadrature amplitude modulation (QAM) digital-to-analog converter (DAC) FMC module or daughtercard. This pin-out satisfies a QAM DAC that requires 58 LVDS data output pairs, one LVDS input clock pair, and three low-voltage differential signaling (LVDS) control pairs from the FPGA device. These pins also have the option to be used as single-ended I/O pins.

The VCCIO supply for the FMC A and FMC B banks provide a variable voltage of 1.2V - 1.8V. The default voltage value is 1.8V.

However, for device safety concerns, a jumper is available for you to connect this bank to the same VCCIO used for the FMC A banks. This allows the VCCIO pins on the FPGA to be tied to a known power. The VCCIO pins also allows you the option to perform a manual check for the module's input voltage before connecting to the FPGA. This is to ensure that the module does not exceed the power supply maximum voltage rating.

Table 33. FMC A Connector Pin Assignments, Schematic Signal Names

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------|-----------------------|-----------------|-----------------------------|
| D1 | FMCA_C2M_PG | — | — |
| H5 | FMCA_CLK_M2C_N0 | AY19 | High Speed Differential I/O |
| G3 | FMCA_CLK_M2C_N1 | BA13 | High Speed Differential I/O |
| H4 | FMCA_CLK_M2C_P0 | AY20 | High Speed Differential I/O |
| G2 | FMCA_CLK_M2C_P1 | BA12 | High Speed Differential I/O |
| C3 | FMCA_DP_C2M_N0 | BC8 | High Speed Differential I/O |
| A23 | FMCA_DP_C2M_N1 | BD6 | High Speed Differential I/O |
| A27 | FMCA_DP_C2M_N2 | BB6 | High Speed Differential I/O |
| A31 | FMCA_DP_C2M_N3 | BC4 | High Speed Differential I/O |
| A35 | FMCA_DP_C2M_N4 | BB2 | High Speed Differential I/O |
| A39 | FMCA_DP_C2M_N5 | BA4 | High Speed Differential I/O |
| B37 | FMCA_DP_C2M_N6 | AY2 | High Speed Differential I/O |
| B33 | FMCA_DP_C2M_N7 | AW4 | High Speed Differential I/O |
| B29 | FMCA_DP_C2M_N8 | AV2 | High Speed Differential I/O |
| B25 | FMCA_DP_C2M_N9 | AU4 | High Speed Differential I/O |
| <i>continued...</i> | | | |

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------|-----------------------|-----------------|-----------------------------|
| K23 | FMCA_DP_C2M_N10 | AT2 | High Speed Differential I/O |
| K26 | FMCA_DP_C2M_N11 | AR4 | High Speed Differential I/O |
| K29 | FMCA_DP_C2M_N12 | AP2 | High Speed Differential I/O |
| K32 | FMCA_DP_C2M_N13 | AM2 | High Speed Differential I/O |
| K35 | FMCA_DP_C2M_N14 | AK2 | High Speed Differential I/O |
| K38 | FMCA_DP_C2M_N15 | AH2 | High Speed Differential I/O |
| C2 | FMCA_DP_C2M_P0 | BC7 | High Speed Differential I/O |
| A22 | FMCA_DP_C2M_P1 | BD5 | High Speed Differential I/O |
| A26 | FMCA_DP_C2M_P2 | BB5 | High Speed Differential I/O |
| A30 | FMCA_DP_C2M_P3 | BC3 | High Speed Differential I/O |
| A34 | FMCA_DP_C2M_P4 | BB1 | High Speed Differential I/O |
| A38 | FMCA_DP_C2M_P5 | BA3 | High Speed Differential I/O |
| B36 | FMCA_DP_C2M_P6 | AY1 | High Speed Differential I/O |
| B32 | FMCA_DP_C2M_P7 | AW3 | High Speed Differential I/O |
| B28 | FMCA_DP_C2M_P8 | AV1 | High Speed Differential I/O |
| B24 | FMCA_DP_C2M_P9 | AU3 | High Speed Differential I/O |
| K22 | FMCA_DP_C2M_P10 | AT1 | High Speed Differential I/O |
| K25 | FMCA_DP_C2M_P11 | AR3 | High Speed Differential I/O |
| K28 | FMCA_DP_C2M_P12 | AP1 | High Speed Differential I/O |
| K31 | FMCA_DP_C2M_P13 | AM1 | High Speed Differential I/O |
| K34 | FMCA_DP_C2M_P14 | AK1 | High Speed Differential I/O |
| K37 | FMCA_DP_C2M_P15 | AH1 | High Speed Differential I/O |
| C7 | FMCA_DP_M2C_N0 | AW8 | High Speed Differential I/O |
| <i>continued...</i> | | | |

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------|-----------------------|-----------------|-----------------------------|
| A3 | FMCA_DP_M2C_N1 | BA8 | High Speed Differential I/O |
| A7 | FMCA_DP_M2C_N2 | AY6 | High Speed Differential I/O |
| A11 | FMCA_DP_M2C_N3 | AV6 | High Speed Differential I/O |
| A15 | FMCA_DP_M2C_N4 | AT6 | High Speed Differential I/O |
| A19 | FMCA_DP_M2C_N5 | AP6 | High Speed Differential I/O |
| B17 | FMCA_DP_M2C_N6 | AN4 | High Speed Differential I/O |
| B13 | FMCA_DP_M2C_N7 | AM6 | High Speed Differential I/O |
| B9 | FMCA_DP_M2C_N8 | AL4 | High Speed Differential I/O |
| B5 | FMCA_DP_M2C_N9 | AK6 | High Speed Differential I/O |
| K5 | FMCA_DP_M2C_N10 | AJ4 | High Speed Differential I/O |
| K8 | FMCA_DP_M2C_N11 | AH6 | High Speed Differential I/O |
| K11 | FMCA_DP_M2C_N12 | AG4 | High Speed Differential I/O |
| K14 | FMCA_DP_M2C_N13 | AF6 | High Speed Differential I/O |
| K17 | FMCA_DP_M2C_N14 | AE4 | High Speed Differential I/O |
| K20 | FMCA_DP_M2C_N15 | AD6 | High Speed Differential I/O |
| C6 | FMCA_DP_M2C_P0 | AW7 | High Speed Differential I/O |
| A2 | FMCA_DP_M2C_P1 | BA7 | High Speed Differential I/O |
| A6 | FMCA_DP_M2C_P2 | AY5 | High Speed Differential I/O |
| A10 | FMCA_DP_M2C_P3 | AV5 | High Speed Differential I/O |
| A14 | FMCA_DP_M2C_P4 | AT5 | High Speed Differential I/O |
| A18 | FMCA_DP_M2C_P5 | AP5 | High Speed Differential I/O |
| B16 | FMCA_DP_M2C_P6 | AN3 | High Speed Differential I/O |
| B12 | FMCA_DP_M2C_P7 | AM5 | High Speed Differential I/O |
| <i>continued...</i> | | | |

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|-----------------------------|
| B8 | FMCA_DP_M2C_P8 | AL3 | High Speed Differential I/O |
| B4 | FMCA_DP_M2C_P9 | AK5 | High Speed Differential I/O |
| K4 | FMCA_DP_M2C_P10 | AJ3 | High Speed Differential I/O |
| K7 | FMCA_DP_M2C_P11 | AH5 | High Speed Differential I/O |
| K10 | FMCA_DP_M2C_P12 | AG3 | High Speed Differential I/O |
| K13 | FMCA_DP_M2C_P13 | AF5 | High Speed Differential I/O |
| K16 | FMCA_DP_M2C_P14 | AE3 | High Speed Differential I/O |
| K19 | FMCA_DP_M2C_P15 | AD5 | High Speed Differential I/O |
| C34 | FMCA_GA0 | BC16 | 1.8 V |
| D35 | FMCA_GA1 | BD16 | 1.8 V |
| D5 | FMCA_GBTCLK_M2C_N0 | AL7 | LVDS |
| B21 | FMCA_GBTCLK_M2C_N1 | AJ7 | LVDS |
| D4 | FMCA_GBTCLK_M2C_P0 | AL8 | LVDS |
| B20 | FMCA_GBTCLK_M2C_P1 | AJ8 | LVDS |
| D34 | FMCA_JTAG_RST | — | — |
| D29 | FMCA_JTAG_TCK | — | — |
| D30 | FMCA_JTAG_TDI | — | — |
| D31 | FMCA_JTAG_TDO | — | — |
| D33 | FMCA_JTAG_TMS | — | — |
| G7 | FMCA_LA_RX_CLK_N0 | AU15 | LVDS |
| D9 | FMCA_LA_RX_CLK_N1 | AR11 | LVDS |
| G6 | FMCA_LA_RX_CLK_P0 | AV15 | LVDS |
| D8 | FMCA_LA_RX_CLK_P1 | AT10 | LVDS |
| G10 | FMCA_LA_RX_N0 | AR19 | LVDS |
| C11 | FMCA_LA_RX_N1 | AW14 | LVDS |
| G13 | FMCA_LA_RX_N2 | AN19 | LVDS |
| C15 | FMCA_LA_RX_N3 | AT15 | LVDS |
| G16 | FMCA_LA_RX_N4 | AP16 | LVDS |
| C19 | FMCA_LA_RX_N5 | AV18 | LVDS |
| G19 | FMCA_LA_RX_N6 | AU13 | LVDS |
| C23 | FMCA_LA_RX_N7 | AV21 | LVDS |

continued...

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|---------------------|
| G22 | FMCA_LA_RX_N8 | AT8 | LVDS |
| G25 | FMCA_LA_RX_N9 | AY12 | LVDS |
| G28 | FMCA_LA_RX_N10 | AY14 | LVDS |
| C27 | FMCA_LA_RX_N11 | AR21 | LVDS |
| G31 | FMCA_LA_RX_N12 | BA14 | LVDS |
| G34 | FMCA_LA_RX_N13 | BB18 | LVDS |
| G37 | FMCA_LA_RX_N14 | AW17 | LVDS |
| G9 | FMCA_LA_RX_P0 | AR20 | LVDS |
| C10 | FMCA_LA_RX_P1 | AV14 | LVDS |
| G12 | FMCA_LA_RX_P2 | AP18 | LVDS |
| C14 | FMCA_LA_RX_P3 | AR15 | LVDS |
| G15 | FMCA_LA_RX_P4 | AR16 | LVDS |
| C18 | FMCA_LA_RX_P5 | AW18 | LVDS |
| G18 | FMCA_LA_RX_P6 | AT13 | LVDS |
| C22 | FMCA_LA_RX_P7 | AU21 | LVDS |
| G21 | FMCA_LA_RX_P8 | AU8 | LVDS |
| G24 | FMCA_LA_RX_P9 | AW12 | LVDS |
| G27 | FMCA_LA_RX_P10 | AY15 | LVDS |
| C26 | FMCA_LA_RX_P11 | AP21 | LVDS |
| G30 | FMCA_LA_RX_P12 | BA15 | LVDS |
| G33 | FMCA_LA_RX_P13 | BB17 | LVDS |
| G36 | FMCA_LA_RX_P14 | AY17 | LVDS |
| H8 | FMCA_LA_TX_N0 | AT22 | LVDS |
| H11 | FMCA_LA_TX_N1 | AP19 | LVDS |
| D12 | FMCA_LA_TX_N2 | AW11 | LVDS |
| H14 | FMCA_LA_TX_N3 | AU17 | LVDS |
| D15 | FMCA_LA_TX_N4 | AV13 | LVDS |
| H17 | FMCA_LA_TX_N5 | AR14 | LVDS |
| D18 | FMCA_LA_TX_N6 | AP17 | LVDS |
| H20 | FMCA_LA_TX_N7 | AT9 | LVDS |
| D21 | FMCA_LA_TX_N8 | AW19 | LVDS |
| H23 | FMCA_LA_TX_N9 | AU12 | LVDS |
| H26 | FMCA_LA_TX_N10 | AY11 | LVDS |
| D24 | FMCA_LA_TX_N11 | AT18 | LVDS |
| H29 | FMCA_LA_TX_N12 | BC15 | LVDS |
| | | | <i>continued...</i> |

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|-----------------|-----------------------|-----------------|--------------|
| D27 | FMCA_LA_TX_N13 | AT20 | LVDS |
| H32 | FMCA_LA_TX_N14 | AW16 | LVDS |
| H35 | FMCA_LA_TX_N15 | BD18 | LVDS |
| H38 | FMCA_LA_TX_N16 | AU20 | LVDS |
| H7 | FMCA_LA_TX_P0 | AR22 | LVDS |
| H10 | FMCA_LA_TX_P1 | AN20 | LVDS |
| D11 | FMCA_LA_TX_P2 | AV11 | LVDS |
| H13 | FMCA_LA_TX_P3 | AT17 | LVDS |
| D14 | FMCA_LA_TX_P4 | AW13 | LVDS |
| H16 | FMCA_LA_TX_P5 | AT14 | LVDS |
| D17 | FMCA_LA_TX_P6 | AR17 | LVDS |
| H19 | FMCA_LA_TX_P7 | AR9 | LVDS |
| D20 | FMCA_LA_TX_P8 | AV19 | LVDS |
| H22 | FMCA_LA_TX_P9 | AU11 | LVDS |
| H25 | FMCA_LA_TX_P10 | AY10 | LVDS |
| D23 | FMCA_LA_TX_P11 | AU18 | LVDS |
| H28 | FMCA_LA_TX_P12 | BB15 | LVDS |
| D26 | FMCA_LA_TX_P13 | AT19 | LVDS |
| H31 | FMCA_LA_TX_P14 | AY16 | LVDS |
| H34 | FMCA_LA_TX_P15 | BC18 | LVDS |
| H37 | FMCA_LA_TX_P16 | AV20 | LVDS |
| F1 | FMCA_M2C_PG | — | |
| H2 | FMCA_PRSNTN | P16 | 1.8 V |
| C30 | FMCA_SCL | AU10 | 1.8 V |
| C31 | FMCA_SDA | AV10 | 1.8 V |
| J39 | VIO_B_M2C | — | — |
| K40 | VIO_B_M2C | — | — |
| K1 | VREF_B_M2C | — | — |
| H1 | VREF_FMCA | — | — |

Table 34. FMC B Connector Pin Assignments, Schematic Signal Names

| FMCB Connector Pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------------|-----------------------|-----------------|-----------------------------|
| D1 | FMCB_C2M_PG | — | — |
| H5 | FMCB_CLK_M2C_N0 | K12 | High Speed Differential I/O |
| <i>continued...</i> | | | |

| FMCB Connector Pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------------|-----------------------|-----------------|-----------------------------|
| G3 | FMCB_CLK_M2C_N1 | G17 | High Speed Differential I/O |
| H4 | FMCB_CLK_M2C_P0 | J12 | High Speed Differential I/O |
| G2 | FMCB_CLK_M2C_P1 | F17 | High Speed Differential I/O |
| C3 | FMCB_DP_C2M_N0 | AB2 | High Speed Differential I/O |
| A23 | FMCB_DP_C2M_N1 | Y2 | High Speed Differential I/O |
| A27 | FMCB_DP_C2M_N2 | V2 | High Speed Differential I/O |
| A31 | FMCB_DP_C2M_N3 | T2 | High Speed Differential I/O |
| A35 | FMCB_DP_C2M_N4 | P2 | High Speed Differential I/O |
| A39 | FMCB_DP_C2M_N5 | M2 | High Speed Differential I/O |
| B37 | FMCB_DP_C2M_N6 | K2 | High Speed Differential I/O |
| B33 | FMCB_DP_C2M_N7 | J4 | High Speed Differential I/O |
| B29 | FMCB_DP_C2M_N8 | H2 | High Speed Differential I/O |
| B25 | FMCB_DP_C2M_N9 | G4 | High Speed Differential I/O |
| K23 | FMCB_DP_C2M_N10 | F2 | High Speed Differential I/O |
| K26 | FMCB_DP_C2M_N11 | E4 | High Speed Differential I/O |
| K29 | FMCB_DP_C2M_N12 | D2 | High Speed Differential I/O |
| K32 | FMCB_DP_C2M_N13 | C4 | High Speed Differential I/O |
| K35 | FMCB_DP_C2M_N14 | B2 | High Speed Differential I/O |
| K38 | FMCB_DP_C2M_N15 | A4 | High Speed Differential I/O |
| C2 | FMCB_DP_C2M_P0 | AB1 | High Speed Differential I/O |
| A22 | FMCB_DP_C2M_P1 | Y1 | High Speed Differential I/O |
| A26 | FMCB_DP_C2M_P2 | V1 | High Speed Differential I/O |
| A30 | FMCB_DP_C2M_P3 | T1 | High Speed Differential I/O |
| <i>continued...</i> | | | |

| FMCB Connector Pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------------|-----------------------|-----------------|-----------------------------|
| A34 | FMCB_DP_C2M_P4 | P1 | High Speed Differential I/O |
| A38 | FMCB_DP_C2M_P5 | M1 | High Speed Differential I/O |
| B36 | FMCB_DP_C2M_P6 | K12 | High Speed Differential I/O |
| B32 | FMCB_DP_C2M_P7 | J3 | High Speed Differential I/O |
| B28 | FMCB_DP_C2M_P8 | H1 | High Speed Differential I/O |
| B24 | FMCB_DP_C2M_P9 | G3 | High Speed Differential I/O |
| K22 | FMCB_DP_C2M_P10 | F1 | High Speed Differential I/O |
| K25 | FMCB_DP_C2M_P11 | E3 | High Speed Differential I/O |
| K28 | FMCB_DP_C2M_P12 | D1 | High Speed Differential I/O |
| K31 | FMCB_DP_C2M_P13 | C3 | High Speed Differential I/O |
| K34 | FMCB_DP_C2M_P14 | B1 | High Speed Differential I/O |
| K37 | FMCB_DP_C2M_P15 | A3 | High Speed Differential I/O |
| C7 | FMCB_DP_M2C_N0 | AA4 | High Speed Differential I/O |
| A3 | FMCB_DP_M2C_N1 | W4 | High Speed Differential I/O |
| A7 | FMCB_DP_M2C_N2 | Y6 | High Speed Differential I/O |
| A11 | FMCB_DP_M2C_N3 | V6 | High Speed Differential I/O |
| A15 | FMCB_DP_M2C_N4 | U4 | High Speed Differential I/O |
| A19 | FMCB_DP_M2C_N5 | T6 | High Speed Differential I/O |
| B17 | FMCB_DP_M2C_N6 | R4 | High Speed Differential I/O |
| B13 | FMCB_DP_M2C_N7 | P6 | High Speed Differential I/O |
| B9 | FMCB_DP_M2C_N8 | N4 | High Speed Differential I/O |
| B5 | FMCB_DP_M2C_N9 | M6 | High Speed Differential I/O |
| K5 | FMCB_DP_M2C_N10 | L4 | High Speed Differential I/O |
| <i>continued...</i> | | | |

| FMCB Connector Pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------------|-----------------------|-----------------|-----------------------------|
| K8 | FMCB_DP_M2C_N11 | K6 | High Speed Differential I/O |
| K11 | FMCB_DP_M2C_N12 | H6 | High Speed Differential I/O |
| K14 | FMCB_DP_M2C_N13 | G8 | High Speed Differential I/O |
| K17 | FMCB_DP_M2C_N14 | F6 | High Speed Differential I/O |
| K20 | FMCB_DP_M2C_N15 | E8 | High Speed Differential I/O |
| C6 | FMCB_DP_M2C_P0 | AA3 | High Speed Differential I/O |
| A2 | FMCB_DP_M2C_P1 | W3 | High Speed Differential I/O |
| A6 | FMCB_DP_M2C_P2 | Y5 | High Speed Differential I/O |
| A10 | FMCB_DP_M2C_P3 | V5 | High Speed Differential I/O |
| A14 | FMCB_DP_M2C_P4 | U3 | High Speed Differential I/O |
| A18 | FMCB_DP_M2C_P5 | T5 | High Speed Differential I/O |
| B16 | FMCB_DP_M2C_P6 | R3 | High Speed Differential I/O |
| B12 | FMCB_DP_M2C_P7 | P5 | High Speed Differential I/O |
| B8 | FMCB_DP_M2C_P8 | N3 | High Speed Differential I/O |
| B4 | FMCB_DP_M2C_P9 | M5 | High Speed Differential I/O |
| K4 | FMCB_DP_M2C_P10 | L3 | High Speed Differential I/O |
| K7 | FMCB_DP_M2C_P11 | K5 | High Speed Differential I/O |
| K10 | FMCB_DP_M2C_P12 | H5 | High Speed Differential I/O |
| K13 | FMCB_DP_M2C_P13 | G7 | High Speed Differential I/O |
| K16 | FMCB_DP_M2C_P14 | F5 | High Speed Differential I/O |
| K19 | FMCB_DP_M2C_P15 | E7 | High Speed Differential I/O |
| C34 | FMCB_GA0 | K22 | 1.8 V |
| D35 | FMCB_GA1 | L22 | 1.8 V |
| D5 | FMCB_GBTCLK_M2C_N0 | W7 | LVDS |
| <i>continued...</i> | | | |

| FMCB Connector Pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------------|-----------------------|-----------------|--------------|
| B21 | FMCB_GBTCLK_M2C_N1 | U7 | LVDS |
| D4 | FMCB_GBTCLK_M2C_P0 | W8 | LVDS |
| B20 | FMCB_GBTCLK_M2C_P1 | U8 | LVDS |
| D34 | FMCB_JTAG_RST | — | LVDS |
| D29 | FMCB_JTAG_TCK | — | LVDS |
| D30 | FMCB_JTAG_TDI | — | LVDS |
| D31 | FMCB_JTAG_TDO | — | LVDS |
| D33 | FMCB_JTAG_TMS | — | LVDS |
| G7 | FMCB_LA_RX_CLK_N0 | C10 | LVDS |
| D9 | FMCB_LA_RX_CLK_N1 | F18 | LVDS |
| G6 | FMCB_LA_RX_CLK_P0 | C11 | LVDS |
| D8 | FMCB_LA_RX_CLK_P1 | G18 | LVDS |
| G10 | FMCB_LA_RX_N0 | D16 | LVDS |
| C11 | FMCB_LA_RX_N1 | H21 | LVDS |
| G13 | FMCB_LA_RX_N2 | B13 | LVDS |
| C15 | FMCB_LA_RX_N3 | B18 | LVDS |
| G16 | FMCB_LA_RX_N4 | D11 | LVDS |
| C19 | FMCB_LA_RX_N5 | C16 | LVDS |
| G19 | FMCB_LA_RX_N6 | F12 | LVDS |
| C23 | FMCB_LA_RX_N7 | G12 | LVDS |
| G22 | FMCB_LA_RX_N8 | G20 | LVDS |
| G25 | FMCB_LA_RX_N9 | H18 | LVDS |
| G28 | FMCB_LA_RX_N10 | L13 | LVDS |
| C27 | FMCB_LA_RX_N11 | J14 | LVDS |
| G31 | FMCB_LA_RX_N12 | M17 | LVDS |
| G34 | FMCB_LA_RX_N13 | M18 | LVDS |
| G37 | FMCB_LA_RX_N14 | M20 | LVDS |
| G9 | FMCB_LA_RX_P0 | D17 | LVDS |
| C10 | FMCB_LA_RX_P1 | G21 | LVDS |
| G12 | FMCB_LA_RX_P2 | A13 | LVDS |
| C14 | FMCB_LA_RX_P3 | A18 | LVDS |
| G15 | FMCB_LA_RX_P4 | D12 | LVDS |
| C18 | FMCB_LA_RX_P5 | B16 | LVDS |
| G18 | FMCB_LA_RX_P6 | E12 | LVDS |
| C22 | FMCB_LA_RX_P7 | G11 | LVDS |

continued...

| FMCB Connector Pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------------|-----------------------|-----------------|---------------------|
| G21 | FMCB_LA_RX_P8 | H20 | LVDS |
| G24 | FMCB_LA_RX_P9 | H19 | LVDS |
| G27 | FMCB_LA_RX_P10 | M12 | LVDS |
| C26 | FMCB_LA_RX_P11 | K14 | LVDS |
| G30 | FMCB_LA_RX_P12 | M16 | LVDS |
| G33 | FMCB_LA_RX_P13 | L18 | LVDS |
| G36 | FMCB_LA_RX_P14 | M21 | LVDS |
| H8 | FMCB_LA_TX_N0 | B17 | LVDS |
| H11 | FMCB_LA_TX_N1 | B15 | LVDS |
| D12 | FMCB_LA_TX_N2 | K19 | LVDS |
| H14 | FMCB_LA_TX_N3 | C13 | LVDS |
| D15 | FMCB_LA_TX_N4 | A14 | LVDS |
| H17 | FMCB_LA_TX_N5 | E10 | LVDS |
| D18 | FMCB_LA_TX_N6 | A12 | LVDS |
| H20 | FMCB_LA_TX_N7 | F10 | LVDS |
| D21 | FMCB_LA_TX_N8 | G13 | LVDS |
| H23 | FMCB_LA_TX_N9 | H10 | LVDS |
| H26 | FMCB_LA_TX_N10 | K17 | LVDS |
| D24 | FMCB_LA_TX_N11 | J13 | LVDS |
| H29 | FMCB_LA_TX_N12 | L14 | LVDS |
| D27 | FMCB_LA_TX_N13 | N13 | LVDS |
| H32 | FMCB_LA_TX_N14 | L19 | LVDS |
| H35 | FMCB_LA_TX_N15 | K21 | LVDS |
| H38 | FMCB_LA_TX_N16 | J21 | LVDS |
| H7 | FMCB_LA_TX_P0 | A17 | LVDS |
| H10 | FMCB_LA_TX_P1 | C15 | LVDS |
| D11 | FMCB_LA_TX_P2 | J19 | LVDS |
| H13 | FMCB_LA_TX_P3 | D13 | LVDS |
| D14 | FMCB_LA_TX_P4 | A15 | LVDS |
| H16 | FMCB_LA_TX_P5 | E11 | LVDS |
| D17 | FMCB_LA_TX_P6 | B12 | LVDS |
| H19 | FMCB_LA_TX_P7 | G10 | LVDS |
| D20 | FMCB_LA_TX_P8 | F13 | LVDS |
| H22 | FMCB_LA_TX_P9 | H11 | LVDS |
| H25 | FMCB_LA_TX_P10 | K16 | LVDS |
| | | | <i>continued...</i> |

| FMCB Connector Pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard |
|---------------------------|-----------------------|-----------------|--------------|
| D23 | FMCB_LA_TX_P11 | H13 | LVDS |
| H28 | FMCB_LA_TX_P12 | M13 | LVDS |
| D26 | FMCB_LA_TX_P13 | M15 | LVDS |
| H31 | FMCB_LA_TX_P14 | K20 | LVDS |
| H34 | FMCB_LA_TX_P15 | L20 | LVDS |
| H37 | FMCB_LA_TX_P16 | J22 | LVDS |
| F1 | FMCB_M2C_PG | — | — |
| H2 | FMCB_PRSENTN | P17 | 1.8 V |
| C30 | FMCB_SCL | J17 | 1.8 V |
| C31 | FMCB_SDA | J16 | 1.8 V |
| J39 | VIO_B_M2C | — | — |
| K40 | VIO_B_M2C | — | — |
| K1 | VREF_B_M2C | — | — |
| H1 | VREF_FMCB | — | — |

Note: The FMC port B has the same pin assignments as port A but on a different board reference designation. For example, the pin assignments for FMCA_LA_TX_P1 is J1.H10 and FMCB_LA_TX_P1 is J2.H10.

6.7.5. QSFP

The Arria 10 GX FPGA development board includes a QSFP module.

Table 35. QSFP Pin Assignments, Schematic Signal Names, and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------|-----------------------|-----------------|-----------------------------|--------------------------|
| 28 | QSFP_3P3V_INTERRUPT_N | AL34 | 1.8 V | QSFP interrupt |
| 31 | QSFP_3P3V_LP_MODE | AK34 | 1.8 V | QSFP low power mode |
| 27 | QSFP_3P3V_MOD_PRSN | AU36 | 1.8 V | Module present |
| 8 | QSFP_3P3V_MOD_SELN | AU35 | 1.8 V | Module select |
| 9 | QSFP_3P3V_RSTN | AV35 | 1.8 V | Module reset |
| 11 | QSFP_3P3V_SCL | AV34 | 1.8 V | QSFP serial 2-wire clock |
| 12 | QSFP_3P3V_SDA | AU31 | 1.8 V | QSFP serial 2-wire data |
| 18 | QSFP_RX_N0 | R41 | High Speed Differential I/O | QSFP transmitter data |
| 21 | QSFP_RX_N1 | P39 | High Speed Differential I/O | QSFP transmitter data |
| 15 | QSFP_RX_N2 | M39 | High Speed Differential I/O | QSFP transmitter data |
| 24 | QSFP_RX_N3 | L41 | High Speed Differential I/O | QSFP transmitter data |
| 17 | QSFP_RX_P0 | R42 | High Speed Differential I/O | QSFP transmitter data |
| 22 | QSFP_RX_P1 | P40 | High Speed Differential I/O | QSFP transmitter data |
| 14 | QSFP_RX_P2 | M40 | High Speed Differential I/O | QSFP transmitter data |
| 25 | QSFP_RX_P3 | L42 | High Speed Differential I/O | QSFP transmitter data |
| 37 | QSFP_TX_N0 | K43 | High Speed Differential I/O | QSFP transmitter data |
| 2 | QSFP_TX_N1 | J41 | High Speed Differential I/O | QSFP transmitter data |
| 34 | QSFP_TX_N2 | G41 | High Speed Differential I/O | QSFP transmitter data |
| 5 | QSFP_TX_N3 | F43 | High Speed Differential I/O | QSFP transmitter data |
| 36 | QSFP_TX_P0 | K44 | High Speed Differential I/O | QSFP transmitter data |
| 3 | QSFP_TX_P1 | J42 | High Speed Differential I/O | QSFP transmitter data |
| 33 | QSFP_TX_P2 | G42 | High Speed Differential I/O | QSFP transmitter data |
| 6 | QSFP_TX_P3 | F44 | High Speed Differential I/O | QSFP transmitter data |

6.7.6. SFP+

The Arria 10 GX FPGA development board includes one SFP+ module that uses transceiver channels from the FPGA. This module takes in serial data from the FPGA and transform them into optical signals. The Arria 10 GX FPGA development board includes one SFP+ cage assembly for the SFP+ port that is used by the device.

Table 36. SFP+ Pin Assignments, Schematic Signal Names, and Functions

| Board Reference (J12) | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------------|-----------------------|-----------------|-----------------------------|--------------------------|
| 6 | SFP_3P3V_MOD0_PRSENTN | AT30 | 1.8 V | Module present indicator |
| 7 | SFP_3P3V_RS0 | AN31 | 1.8 V | SFP+ rate select 0 |
| 9 | SFP_3P3V_RS1 | AT34 | 1.8 V | SFP+ rate select 1 |
| 8 | SFP_3P3V_RX_LOS | AU30 | 1.8 V | Signal present indicator |
| 3 | SFP_3P3V_TX_DIS | AR35 | 1.8 V | Transmitter disable |
| 2 | SFP_3P3V_TX_FLT | AT35 | 1.8 V | Transmitter fault |
| 12 | SFP_RX_N | AA41 | High Speed Differential I/O | Receiver data |
| 13 | SFP_RX_P | AA42 | High Speed Differential I/O | Receiver data |
| 5 | SFP_SCL | — | High Speed Differential I/O | Serial 2-wire clock |
| 4 | SFP_SDA | — | High Speed Differential I/O | Serial 2-wire data |
| 19 | SFP_TX_N | AB43 | High Speed Differential I/O | Transmitter data |
| 18 | SFP_TX_P | AB44 | High Speed Differential I/O | Transmitter data |

6.7.7. I²C

I²C supports communication between integrated circuits on a board. It is a simple two-wire bus that consists of a serial data line (SDA) and a serial clock (SCL). The MAX V and Arria 10 devices use the I²C for reading and writing to the character LCD. You can use the Arria 10 or MAX V as the I²C host to access the PLLs and clocks.

Figure 34. I²C Block Diagram

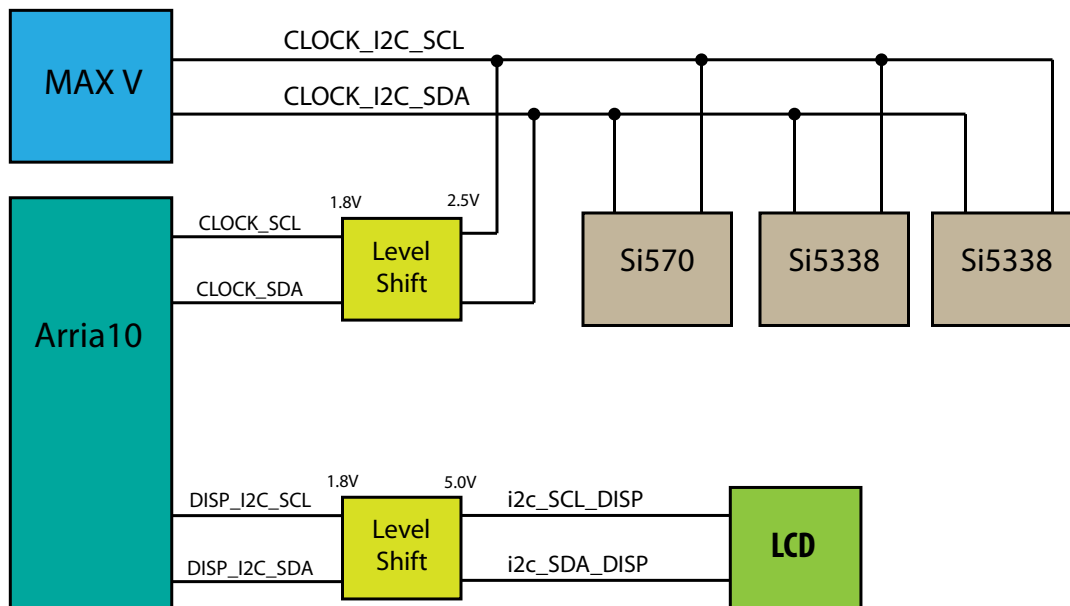


Table 37. MAX V I²C Signals

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|---|
| CLOCK_I2C_SCL | C12 | 2.5 V | I ² C serial clock from MAX V. |
| CLOCK_I2C_SDA | C10 | 2.5 V | I ² C serial data from MAX V. |

Table 38. MAV I²C Level Shifter Signals to Arria 10 FPGA

| Schematic Signal Name | Arria 10 Pin Number | I/O Standard | Description |
|-----------------------|---------------------|--------------|---|
| CLOCK_SCL | AN30 | 1.8 V | Arria 10 FPGA I ² C serial clock from MAX V level shifter. |
| CLOCK_SDA | AV33 | 1.8 V | Arria 10 FPGA I ² C serial data from MAX V level shifter. |

Table 39. Arria 10 I²C Signals

| Schematic Signal Name | Pin Number | I/O Standard | Description |
|-----------------------|------------|--------------|--|
| DISP_I2C_SCL | AW33 | 1.8 V | Arria 10 I ² C serial clock to level shifter. |
| DISP_I2C_SDA | AY34 | 1.8 V | Arria 10 I ² C serial data to level shifter. |

Table 40. Arria 10 I²C Level Shifter to LCD Signals

| Schematic Signal Name | LCD Pin Number | I/O Standard | Description |
|-----------------------|----------------|--------------|---|
| I2C_SCL_DISP | 7 | 5.0 V | LCD I ² C serial clock from Arria 10 FPGA level shifter. |
| I2C_SDA_DISP | 8 | 5.0 V | LCD I ² C serial data from Arria 10 FPGA level shifter. |

6.8. Memory

This section describes the development board's memory interface support and also their signal names, types, and connectivity relative to the FPGA.

6.8.1. Flash

The Arria 10 GX FPGA development board supports two 1 Gb CFI-compatible synchronous flash devices for non-volatile storage of FPGA configuration data, board information, test application data, and user code space. These devices are part of the shared FM bus that connects to the flash memory and MAX V CPLD EPM2210 System Controller.

Table 41. Default Memory Map of two 1-Gb CFI Flash Devices

| Block Description | Size (KB) | Address Range |
|---------------------------|-----------|---------------------------|
| Board test system scratch | 512 | 0x0a10.0000 - 0x0a17.FFFF |
| User software | 14, 336 | 0x0930.0000 - 0x0A0F.FFFF |
| Factory software | 8, 192 | 0x08b0.0000 - 0x092F.FFFF |
| Zips (html, web content) | 8, 192 | 0x0830.0000 - 0x08AF.FFFF |
| User hardware2 | 44, 032 | 0x0580.0000 - 0x082F.FFFF |
| User hardware1 | 44, 032 | 0x02D0.0000 - 0x057F.FFFF |
| Factory hardware | 44, 032 | 0x0020.0000 - 0x02CF.FFFF |
| PFL option bits | 512 | 0x0018.0000 - 0x001F.FFFF |
| Board information | 512 | 0x0010.0000 - 0x0017.FFFF |
| Ethernet option bits | 512 | 0x0008.0000 - 0x000F.FFFF |
| User design reset vector | 512 | 0x0000.0000 - 0x0007.FFFF |

Table 42. Flash Pin Assignments, Schematic Signal Names, and Functions

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------|-----------------------|-----------------|--------------|---------------|
| F6 | FLASH_ADVN | BB22 | 1.8 V | Address valid |
| B4 | FLASH_CEN1 | BB23 | 1.8 V | Chip enable |
| E6 | FLASH_CLK | BB25 | 1.8 V | Clock |
| F8 | FLASH_OEN | BC26 | 1.8 V | Output enable |
| F7 | FLASH_RDYBSYN1 | AV23 | 1.8 V | Ready |
| D4 | FLASH_RESETN | BA23 | 1.8 V | Reset |
| G8 | FLASH_WEN | BD26 | 1.8 V | Write enable |
| C6 | FLASH_WPN | — | 1.8 V | Write protect |
| A1 | FM_A1 | AM11 | 1.8 V | Address bus |
| B1 | FM_A2 | AM12 | 1.8 V | Address bus |
| C1 | FM_A3 | AL12 | 1.8 V | Address bus |
| D1 | FM_A4 | AN13 | 1.8 V | Address bus |

continued...

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------|-----------------------|-----------------|--------------|-------------|
| D2 | FM_A5 | AM13 | 1.8 V | Address bus |
| A2 | FM_A6 | AE12 | 1.8 V | Address bus |
| C2 | FM_A7 | AN15 | 1.8 V | Address bus |
| A3 | FM_A8 | AL10 | 1.8 V | Address bus |
| B3 | FM_A9 | AR10 | 1.8 V | Address bus |
| C3 | FM_A10 | AP11 | 1.8 V | Address bus |
| D3 | FM_A11 | AL13 | 1.8 V | Address bus |
| C4 | FM_A12 | AH11 | 1.8 V | Address bus |
| A5 | FM_A13 | AN14 | 1.8 V | Address bus |
| B5 | FM_A14 | AG11 | 1.8 V | Address bus |
| C5 | FM_A15 | AH10 | 1.8 V | Address bus |
| D7 | FM_A16 | AF14 | 1.8 V | Address bus |
| D8 | FM_A17 | AF15 | 1.8 V | Address bus |
| A7 | FM_A18 | AH14 | 1.8 V | Address bus |
| B7 | FM_A19 | AJ12 | 1.8 V | Address bus |
| C7 | FM_A20 | AJ14 | 1.8 V | Address bus |
| C8 | FM_A21 | AH13 | 1.8 V | Address bus |
| A8 | FM_A22 | AG12 | 1.8 V | Address bus |
| G1 | FM_A23 | AJ13 | 1.8 V | Address bus |
| H8 | FM_A24 | AF12 | 1.8 V | Address bus |
| B6 | FM_A25 | AK14 | 1.8 V | Address bus |
| B8 | FM_A26 | AK11 | 1.8 V | Address bus |
| F2 | FM_D16 | AT25 | 1.8 V | Data bus |
| E2 | FM_D17 | BA19 | 1.8 V | Data bus |
| G3 | FM_D18 | BA20 | 1.8 V | Data bus |
| E4 | FM_D19 | AP24 | 1.8 V | Data bus |
| E5 | FM_D20 | AP23 | 1.8 V | Data bus |
| G5 | FM_D21 | BA18 | 1.8 V | Data bus |
| G6 | FM_D22 | AT24 | 1.8 V | Data bus |
| H7 | FM_D23 | BD19 | 1.8 V | Data bus |
| E1 | FM_D24 | AU23 | 1.8 V | Data bus |
| E3 | FM_D25 | AR24 | 1.8 V | Data bus |
| F3 | FM_D26 | AT23 | 1.8 V | Data bus |
| F4 | FM_D27 | AR25 | 1.8 V | Data bus |
| F5 | FM_D28 | AP22 | 1.8 V | Data bus |

continued...

| Board Reference | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|-----------------|-----------------------|-----------------|--------------|-------------|
| H5 | FM_D29 | BC19 | 1.8 V | Data bus |
| G7 | FM_D30 | AU22 | 1.8 V | Data bus |
| E7 | FM_D31 | BA17 | 1.8 V | Data bus |

6.8.2. Programming the Flash Using Quartus Programmer

You can use the Quartus Programmer to program the flash with your Programmer Object File (.pof).

Ensure the following conditions are met before you proceed:

- The Quartus Programmer and the USB-Blaster II driver are installed on the host computer.
- The micro-USB cable is connected to the FPGA development board.
- Power to the board is on, and no other applications that use the JTAG chain are running.
- The design running in the FPGA does not drive the FM bus.

Execute the steps below to program the Flash

1. Start the Quartus Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Select the flash attached to the MAX V and then click **Change File** and select the path to the desired .pof. If the flash is not detected, configure the FPGA with `<package root directory>\examples\board_test_system\image \<Silicon Type>\dummy.sof` and then go to step 2, refer to **Configuring the FPGA Using Programmer**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to program the selected file to the flash. Programming is complete when the progress bar reaches 100%.

Attention: Using the Quartus Programmer to program a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after programming is complete.

6.9. Board Power Supply

This section describes the Arria 10 GX FPGA development board's power supply. A laptop style DC power supply is provided with the development kit. Use only the supplied power supply. The power supply has an auto sensing input voltage range of 100 ~ 240 VAC and will output 12 VDC power at 16 A to the development board. The 12 VDC input power is then stepped down to various power rails used by the board components.

An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed on a graphical user interface (GUI) that can graph power consumption versus time.

6.9.1. Power Distribution System

The following figure below shows the power distribution system on the A10 FPGA development board. Regulator efficiencies and sharing are reflected in the currents shown, which are at conservative absolute maximum levels.

Figure 35. Power Distribution System Block Diagram (ES Edition)

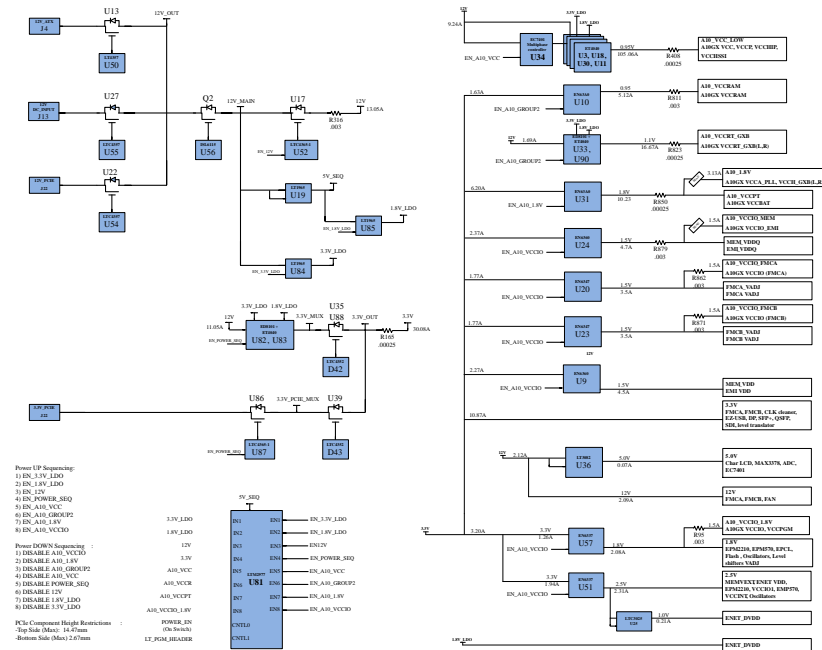
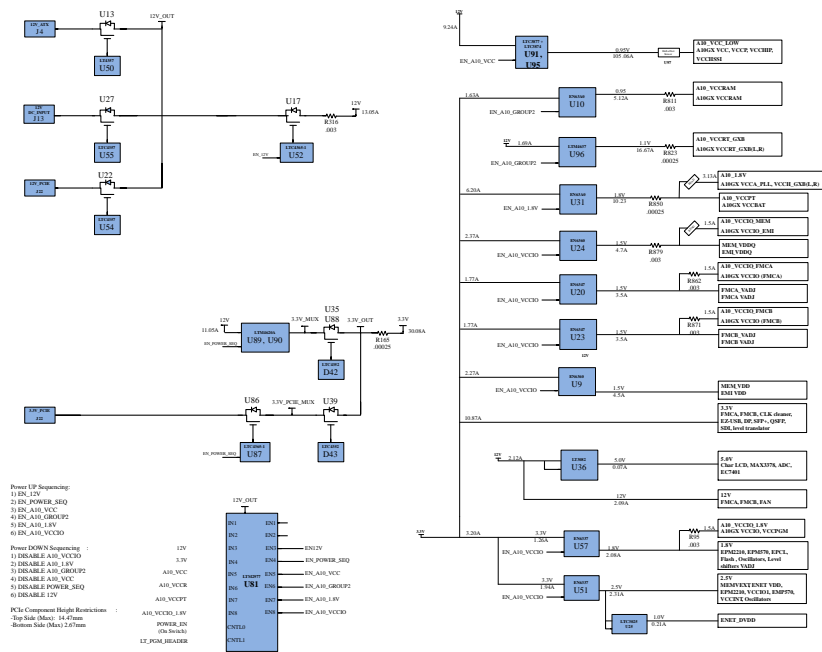


Figure 36. Power Distribution System Block Diagram



6.9.2. Power Measurement

There are 8 power supply rails that have on-board voltage, current, and wattage sense capabilities using 24-bit differential ADC devices. Precision sense resistors split the ADC devices and rails from the primary supply plane for the ADC to measure voltage and current. A SPI bus connects these ADC devices to the MAX V CPLD EPM2210 System Controller as well as the Arria 10 GX FPGA.

6.10. Daughtercards

The Arria 10 development kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to an Arria 10 GX FPGA.

Table 43. Arria 10 FPGA Development Kit Daughtercards

| Memory Type | Transfer Rate (Mbps) | Maximum Frequency (MHz) |
|--------------|----------------------|-------------------------|
| DDR3 | 2,133 | 1,066 |
| DDR4 | 2,666 | 1,333 |
| RLDRAM 3 | 2,400 | 1,200 |
| QDR-IV | 2,133 | 1,066 |
| FMC Loopback | 14,200 | 7,100 |

Related Information

[I/O and High Speed I/O Arria 10 Devices](#)

6.10.1. External Memory Interface

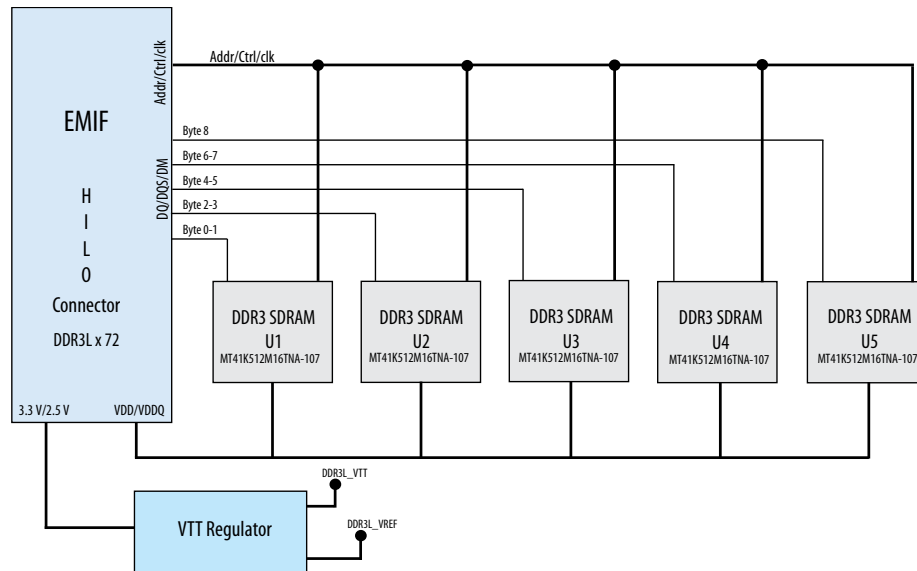
Related Information

Arria 10 FPGA and SoC External Memory Resources

6.10.1.1. DDR3L

The DDR3L x 72 SDRAM (DDR3 Low Voltage)

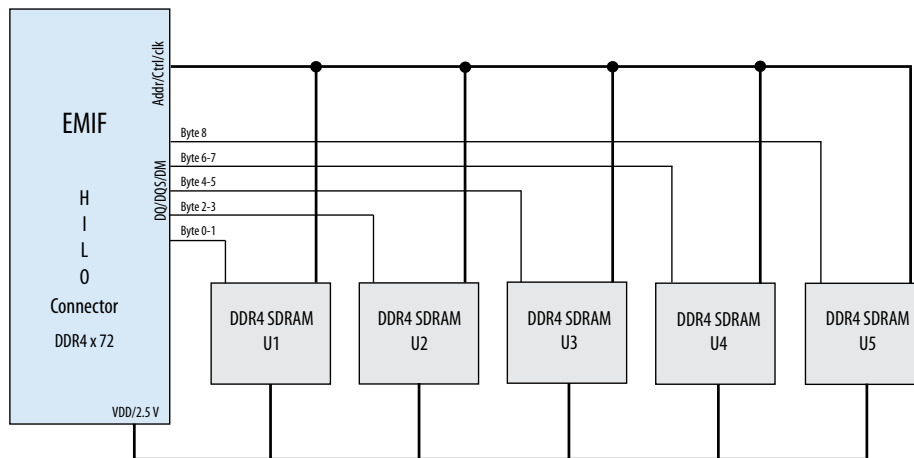
Figure 37. DDR3 Block Diagram



6.10.1.2. DDR4

DDR4 x 72 SDRAM

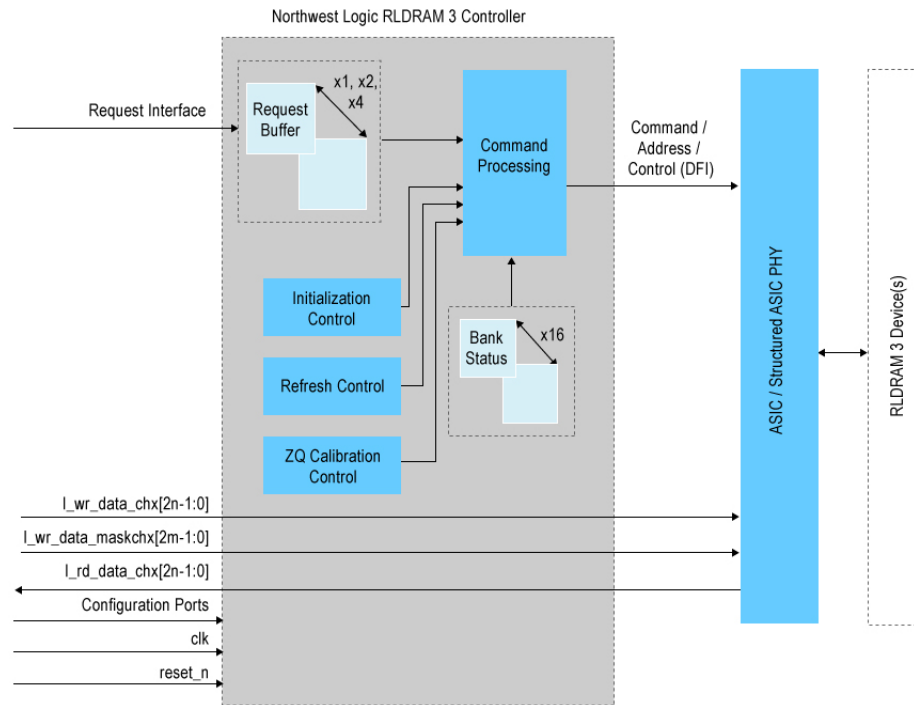
Figure 38. DDR4 Block Diagram



6.10.1.3. RLD RAM 3

The RLD RAM 3 x 36 (reduced latency DRAM) controller is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

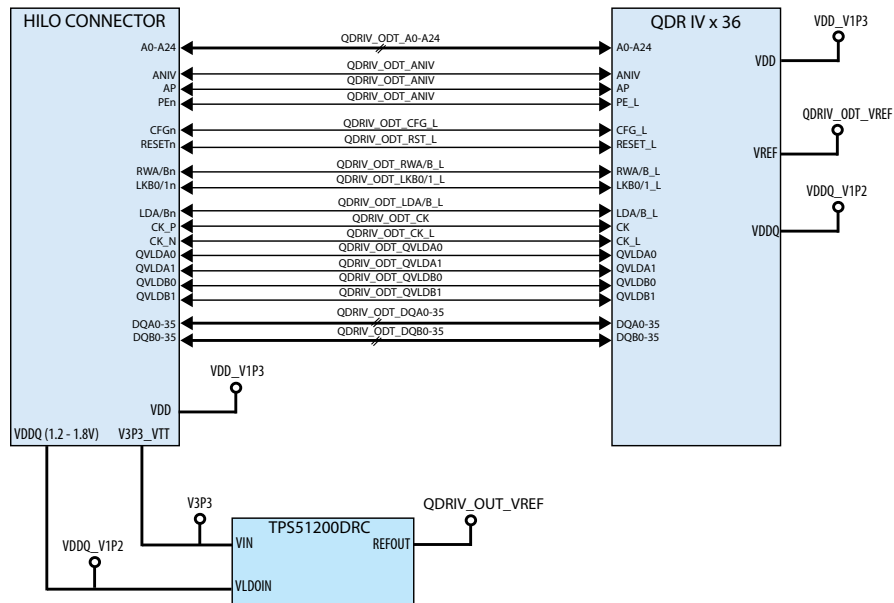
Figure 39. RLD RAM 3 Block Diagram



6.10.1.4. QDR-IV

QDR-IV x 36 SRAM devices enable you to maximize memory bandwidth with separate read and write ports.

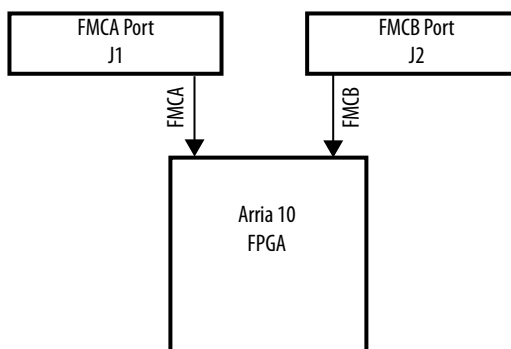
Figure 40. QDR-IV Block Diagram



6.10.1.5. FMC Loopback Card

The Arria 10 FPGA development kit provides two FMC mezzanine interface ports connected to the Arria 10 FPGA for interfacing to Altera FMC add-in boards as shown in the figure below. The Altera FMC interface is mechanically compliant with the Vita57.1 specification for attaching a double width mezzanine module. However, in terms of signal connections, the Altera FMC interface is not fully compliant with the Vita 57.1 specification. Instead, it contains a subset of the Vita57.1 interface signal to the connector as shown in the FMCA and FMCB signal assignments tables.

Figure 41. Arria 10 FPGA Development Kit FMC Block Diagram



The following shows the complete signal connections assigned for each Altera FMC interface at the FMCA port (J1) and FMCB port (J2). For the signal connections to the FPGA device, refer to [Table 33](#) on page 86.

Table 44. FMCA Connector (J1) Signal Assignments

| | K | J | H | G | F | E | D | C | B | A |
|----|-----------------|-----|-----------------|-------------------|-------------|-----|--------------------|----------------|----------------|----------------|
| 1 | NC | GND | VREF_FMCA | GND | FMCA_M2C_PG | GND | FMCA_C2M_PG | GND | NC | GND |
| 2 | GND | NC | FMCA_PRSN_Tn | FMCA_CLK_M2C_P1 | GND | NC | GND | FMCA_DP_C2M_P0 | GND | FMCA_DP_M2C_P1 |
| 3 | GND | NC | GND | FMCA_CLK_M2C_N1 | GND | NC | GND | FMCA_DP_C2M_N0 | GND | FMCA_DP_M2C_N1 |
| 4 | FMCA_DP_M2C_P10 | GND | FMCA_CLK_M2C_P0 | GND | NC | GND | FMCA_GBTCLK_M2C_P0 | GND | FMCA_DP_M2C_P9 | GND |
| 5 | FMCA_DP_M2C_N10 | GND | FMCA_CLK_M2C_N0 | GND | NC | GND | FMCA_GBTCLK_M2C_N0 | GND | FMCA_DP_M2C_N9 | GND |
| 6 | GND | NC | GND | FMCA_LA_RX_CLK_P0 | GND | NC | GND | FMCA_DP_M2C_P0 | GND | FMCA_DP_M2C_P2 |
| 7 | FMCA_DP_M2C_P11 | GND | FMCA_LA_TX_P0 | FMCA_LA_RX_CLK_N0 | NC | NC | GND | FMCA_DP_M2C_N0 | GND | FMCA_DP_M2C_N2 |
| 8 | FMCA_DP_M2C_N11 | GND | FMCA_LA_TX_N0 | GND | NC | GND | FMCA_LA_RX_C_LK_P1 | GND | FMCA_DP_M2C_P8 | GND |
| 9 | GND | NC | GND | FMCA_LA_RX_P0 | GND | NC | FMCA_LA_RX_C_LK_N1 | GND | FMCA_DP_M2C_N8 | GND |
| 10 | FMCA_DP_M2C_P12 | GND | FMCA_LA_TX_P1 | FMCA_LA_RX_N0 | NC | NC | GND | FMCA_LA_RX_P1 | GND | FMCA_DP_M2C_P3 |
| 11 | FMCA_DP_M2C_N12 | GND | FMCA_LA_TX_N1 | GND | NC | GND | FMCA_LA_TX_P2 | FMCA_LA_RX_N1 | GND | FMCA_DP_M2C_N3 |
| 12 | GND | NC | GND | FMCA_LA_RX_P2 | GND | NC | FMCA_LA_TX_N2 | GND | FMCA_DP_M2C_P7 | GND |

continued...

| | K | J | H | G | F | E | D | C | B | A |
|----|-----------------|-----|----------------|----------------|-----|-----|----------------|----------------|--------------------|----------------|
| 13 | FMCA_DP_M2C_P13 | GND | FMCA_LA_TX_P3 | FMCA_LA_RX_N2 | NC | NC | GND | GND | FMCA_DP_M2C_N7 | GND |
| 14 | FMCA_DP_M2C_N13 | GND | FMCA_LA_TX_N3 | GND | NC | GND | FMCA_LA_TX_P4 | FMCA_LA_RX_P3 | GND | FMCA_DP_M2C_P4 |
| 15 | GND | NC | GND | FMCA_LA_RX_P4 | GND | NC | FMCA_LA_TX_N4 | FMCA_LA_RX_N3 | GND | FMCA_DP_M2C_N4 |
| 16 | FMCA_DP_M2C_P14 | GND | FMCA_LA_TX_P5 | FMCA_LA_RX_N4 | NC | NC | GND | GND | FMCA_DP_M2C_P6 | GND |
| 17 | FMCA_DP_M2C_N14 | GND | FMCA_LA_TX_N5 | GND | NC | GND | FMCA_LA_TX_P6 | GND | FMCA_DP_M2C_N6 | GND |
| 18 | GND | NC | GND | FMCA_LA_RX_P6 | GND | NC | FMCA_LA_TX_N6 | FMCA_LA_RX_P5 | GND | FMCA_DP_M2C_P5 |
| 19 | FMCA_DP_M2C_P15 | GND | FMCA_LA_TX_P7 | FMCA_LA_RX_N6 | NC | NC | GND | FMCA_LA_RX_N5 | GND | FMCA_DP_M2C_N5 |
| 20 | FMCA_DP_M2C_N15 | GND | FMCA_LA_TX_N7 | GND | NC | GND | FMCA_LA_TX_P8 | GND | FMCA_GBTCLK_M2C_P1 | GND |
| 21 | GND | NC | GND | FMCA_LA_RX_P8 | GND | NC | FMCA_LA_TX_N8 | GND | FMCA_GBTCLK_M2C_N1 | GND |
| 22 | FMCA_DP_C2M_P10 | GND | FMCA_LA_TX_P9 | FMCA_LA_RX_N8 | NC | NC | GND | FMCA_LA_RX_P7 | GND | FMCA_DP_C2M_P1 |
| 23 | FMCA_DP_C2M_N10 | GND | FMCA_LA_TX_N9 | GND | NC | GND | FMCA_LA_TX_P11 | FMCA_LA_RX_N7 | GND | FMCA_DP_C2M_N1 |
| 24 | GND | NC | GND | FMCA_LA_RX_P9 | GND | NC | FMCA_LA_TX_N11 | GND | FMCA_DP_C2M_P9 | GND |
| 25 | FMCA_DP_C2M_P11 | GND | FMCA_LA_TX_P10 | FMCA_LA_RX_N9 | NC | NC | GND | GND | FMCA_DP_C2M_N9 | GND |
| 26 | FMCA_DP_C2M_N11 | GND | FMCA_LA_TX_N10 | GND | NC | GND | FMCA_LA_TX_P13 | FMCA_LA_RX_P11 | GND | FMCA_DP_C2M_P2 |
| 27 | GND | NC | GND | FMCA_LA_RX_P10 | GND | NC | FMCA_LA_TX_N13 | FMCA_LA_RX_N11 | GND | FMCA_DP_C2M_N2 |
| 28 | FMCA_DP_C2M_P12 | GND | FMCA_LA_TX_P12 | FMCA_LA_RX_N10 | NC | NC | GND | GND | FMCA_DP_C2M_P8 | GND |
| 29 | FMCA_DP_C2M_N12 | GND | FMCA_LA_TX_N12 | GND | NC | GND | FMCA_JTAG_TCK | GND | FMCA_DP_C2M_N8 | GND |
| 30 | GND | NC | GND | FMCA_LA_RX_P12 | GND | NC | FMCA_JTAG_TDI | FMCA_3P3V_SCL | GND | FMCA_DP_C2M_P3 |
| 31 | FMCA_DP_C2M_P13 | GND | FMCA_LA_TX_P14 | FMCA_LA_RX_N12 | NC | NC | FMCA_JTAG_TDO | FMCA_3P3V_SDA | GND | FMCA_DP_C2M_N3 |
| 32 | FMCA_DP_C2M_N13 | GND | FMCA_LA_TX_N14 | GND | NC | GND | 3.3V | GND | FMCA_DP_C2M_P7 | GND |
| 33 | GND | NC | GND | FMCA_LA_RX_P13 | GND | NC | FMCA_JTAG_TMS | GND | FMCA_DP_C2M_N7 | GND |
| 34 | FMCA_DP_C2M_P14 | GND | FMCA_LA_TX_P15 | FMCA_LA_RX_N13 | NC | NC | FMCA_JTAG_RST | FMCA_GA0 | GND | FMCA_DP_C2M_P4 |
| 35 | FMCA_DP_C2M_N14 | GND | FMCA_LA_TX_N15 | GND | NC | GND | FMCA_GA1 | 12V | GND | FMCA_DP_C2M_N4 |
| 36 | GND | NC | GND | FMCA_LA_RX_P14 | GND | NC | 3.3V | GND | FMCA_DP_C2M_P6 | GND |
| 37 | FMCA_DP_C2M_P15 | GND | FMCA_LA_TX_P16 | FMCA_LA_RX_N14 | NC | NC | GND | 12V | FMCA_DP_C2M_N6 | GND |
| 38 | FMCA_DP_C2M_N15 | GND | FMCA_LA_TX_N16 | GND | NC | GND | 3.3V | GND | GND | FMCA_DP_C2M_P5 |

continued...

| | K | J | H | G | F | E | D | C | B | A |
|----|-----|-----|--------------------|--------------------|--------------------|--------------------|---------------|------------------|-----|--------------------|
| 39 | GND | NC | GND | A10_VCCIO_F MCA | GND | A10_VCCI O_FMCA | GND | 3.3V | GND | FMCA_DP_ C2M_N5 |
| 40 | NC | GND | A10_VCCIO_ FMCA | GND | A10_VCCI O_FMCA | GND | 3.3V | GND | NC | GND |
| | | | LPC Connector | LPC Connector | | | HPC Connector | HPC Connector | | |

Table 45. FMCB Connector (J2) Signals Assignments

| | K | J | H | G | F | E | D | C | |
|----|-----------------|-----|-----------------|-------------------|-------------|-----|--------------------|----------------|---------|
| 1 | NC | GND | VREF_FMCB | GND | FMCB_M2C_PG | GND | FMCB_C2M_PG | GND | NC |
| 2 | GND | NC | FMCB_PRSNTrn | FMCB_CLK_M2C_P1 | GND | NC | GND | FMCA_DP_C2M_P0 | GND |
| 3 | GND | NC | GND | FMCB_CLK_M2C_N1 | GND | NC | GND | FMCA_DP_C2M_N0 | GND |
| 4 | FMCB_DP_M2C_P10 | GND | FMCB_CLK_M2C_P0 | GND | NC | GND | FMCB_GBTCLK_M2C_P0 | GND | FMCB_DP |
| 5 | FMCB_DP_M2C_N10 | GND | FMCB_CLK_M2C_N0 | GND | NC | GND | FMCB_GBTCLK_M2C_N0 | GND | FMCB_DP |
| 6 | GND | NC | GND | FMCB_LA_RX_CLK_P0 | GND | NC | GND | FMCA_DP_M2C_P0 | GND |
| 7 | FMCB_DP_M2C_P11 | GND | FMCB_LA_TX_P0 | FMCB_LA_RX_CLK_N0 | NC | NC | GND | FMCA_DP_M2C_N0 | GND |
| 8 | FMCB_DP_M2C_N11 | GND | FMCB_LA_TX_N0 | GND | NC | GND | FMCB_LA_RX_CLK_P1 | GND | FMCB_DP |
| 9 | GND | NC | GND | FMCB_LA_RX_P0 | GND | NC | FMCB_LA_RX_CLK_N1 | GND | FMCB_DP |
| 10 | FMCB_DP_M2C_P12 | GND | FMCB_LA_TX_P1 | FMCB_LA_RX_N0 | NC | NC | GND | FMCB_LA_RX_P1 | GND |
| 11 | FMCB_DP_M2C_N12 | GND | FMCB_LA_TX_N1 | GND | NC | GND | FMCB_LA_TX_P2 | FMCB_LA_RX_N1 | GND |
| 12 | GND | NC | GND | FMCB_LA_RX_P2 | GND | NC | FMCB_LA_TX_N2 | GND | FMCB_DP |
| 13 | FMCB_DP_M2C_P13 | GND | FMCB_LA_TX_P3 | FMCB_LA_RX_N2 | NC | NC | GND | GND | FMCB_DP |
| 14 | FMCB_DP_M2C_N13 | GND | FMCB_LA_TX_N3 | GND | NC | GND | FMCB_LA_TX_P4 | FMCB_LA_RX_P3 | GND |
| 15 | GND | NC | GND | FMCB_LA_RX_P4 | GND | NC | FMCB_LA_TX_N4 | FMCB_LA_RX_N3 | GND |
| 16 | FMCB_DP_M2C_P14 | GND | FMCB_LA_TX_P5 | FMCB_LA_RX_N4 | NC | NC | GND | GND | FMCB_DP |
| 17 | FMCB_DP_M2C_N14 | GND | FMCB_LA_TX_N5 | GND | NC | GND | FMCB_LA_TX_P6 | GND | FMCB_DP |
| 18 | GND | NC | GND | FMCB_LA_RX_P6 | GND | NC | FMCB_LA_TX_N6 | FMCB_LA_RX_P5 | GND |
| 19 | FMCB_DP_M2C_P15 | GND | FMCB_LA_TX_P7 | FMCB_LA_RX_N6 | NC | NC | GND | FMCB_LA_RX_N5 | GND |
| 20 | FMCB_DP_M2C_N15 | GND | FMCB_LA_TX_N7 | GND | NC | GND | FMCB_LA_TX_P8 | GND | FMCB_GB |
| 21 | GND | NC | GND | FMCB_LA_RX_P8 | GND | NC | FMCB_LA_TX_N8 | GND | FMCB_GB |
| 22 | FMCB_DP_C2M_P10 | GND | FMCB_LA_TX_P9 | FMCB_LA_RX_N8 | NC | NC | GND | FMCB_LA_RX_P7 | GND |
| 23 | FMCB_DP_C2M_N10 | GND | FMCB_LA_TX_N9 | GND | NC | GND | FMCB_LA_TX_P11 | FMCB_LA_RX_N7 | GND |
| 24 | GND | NC | GND | FMCB_LA_RX_P9 | GND | NC | FMCB_LA_TX_N11 | GND | FMCB_DP |
| 25 | FMCB_DP_C2M_P11 | GND | FMCB_LA_TX_P10 | FMCB_LA_RX_N9 | NC | NC | GND | GND | FMCB_DP |
| 26 | FMCB_DP_C2M_N11 | GND | FMCB_LA_TX_N10 | GND | NC | GND | FMCB_LA_TX_P13 | FMCB_LA_RX_P11 | GND |
| 27 | GND | NC | GND | FMCB_LA_RX_P10 | GND | NC | FMCB_LA_TX_N13 | FMCB_LA_RX_N11 | GND |
| 28 | FMCB_DP_C2M_P12 | GND | FMCB_LA_TX_P12 | FMCB_LA_RX_N10 | NC | NC | GND | GND | FMCB_DP |
| 29 | FMCB_DP_C2M_N12 | GND | FMCB_LA_TX_N12 | GND | NC | GND | FMCB_JTAG_TCK | GND | FMCB_DP |
| 30 | GND | NC | GND | FMCB_LA_RX_P12 | GND | NC | FMCB_JTAG_TDI | FMCB_3P3V_SCL | GND |
| 31 | FMCB_DP_C2M_P13 | GND | FMCB_LA_TX_P14 | FMCB_LA_RX_N12 | NC | NC | FMCB_JTAG_TDO | FMCB_3P3V_SDA | GND |
| 32 | FMCB_DP_C2M_N13 | GND | FMCB_LA_TX_N14 | GND | NC | GND | 3.3V | GND | FMCB_DP |
| 33 | GND | NC | GND | FMCB_LA_RX_P13 | GND | NC | FMCB_JTAG_TMS | GND | FMCB_DP |
| 34 | FMCB_DP_C2M_P14 | GND | FMCB_LA_TX_P15 | FMCB_LA_RX_N13 | NC | NC | FMCB_JTAG_RST | FMCB_GA0 | GND |

| | K | J | H | G | F | E | D | C | B |
|----|-----------------|-----|----------------|----------------|----------------|----------------|---------------|---------------|-----------|
| 35 | FMCB_DP_C2M_N14 | GND | FMCB_LA_TX_N15 | GND | NC | GND | FMCB_GA1 | 12V | GND |
| 36 | GND | NC | GND | FMCB_LA_RX_P14 | GND | NC | 3.3V | GND | FMCB_DP_C |
| 37 | FMCB_DP_C2M_P15 | GND | FMCB_LA_TX_P16 | FMCB_LA_RX_N14 | NC | NC | GND | 12V | FMCB_DP_C |
| 38 | FMCB_DP_C2M_N15 | GND | FMCB_LA_TX_N16 | GND | NC | GND | 3.3V | GND | GND |
| 39 | GND | NC | GND | A10_VCCIO_FMCB | GND | A10_VCCIO_FMCB | GND | 3.3V | GND |
| 40 | NC | GND | A10_VCCIO_FMCB | GND | A10_VCCIO_FMCB | GND | 3.3V | GND | NC |
| | | | LPC Connector | LPC Connector | | | HPC Connector | HPC Connector | |

6.10.1.5.1. High Pin Count (HBC)

The High Pin Count FMC connections are assigned to columns G and H in both the FMCA (J1) and FMCB (J2) connectors as shown. The HPC signaling follows the Vita57.1 standard.

6.10.1.5.2. Low Pin Count (LPC)

The Low Pin Count FMC connections are assigned to columns C and D in both the FMCA (J1) and FMCB (J2) connectors as shown. The LPC signaling follows the Vita57.1 standard.

A. Additional Information

A.1. Document Revision History for the Intel Arria 10 FPGA Development Kit User Guide

| Document Version | Changes |
|------------------|---|
| 2023.07.12 | <ul style="list-style-type: none"> Retitled the document from <i>Arria 10 FPGA Development Kit User Guide</i> to <i>Intel Arria 10 FPGA Development Kit User Guide</i>. Minor text edits. |
| 2023.07.11 | Updated the supported I/O standard for X1 and X2 in Table: <i>On-Board Oscillators</i> . |
| 2021.03.19 | Updated Board Overview on page 55 [J14 - DDR4 memory (x72) 1200 MHz] |
| 2017.09.21 | Updated contents of FACTORY switch in SW6 DIP Switch Default Settings Table in Default Switch and Jumper Settings on page 12. |
| 2017.08.08 | Added a Caution note to Handling the Board on page 7. |
| 2017.07.25 | <ul style="list-style-type: none"> Updated FMC on page 86 of Board Components. Changed all 1.4V PCML I/O Standard to "High Speed Differential I/O" throughout the User Guide. Updated Development Kit Package on page 9 section to remove references to installer. |
| 2016.05.02 | <ul style="list-style-type: none"> Added "Programming the Flash Using Quartus Programmer" section. Updated the Arria 10 FPGA Development Kit block diagram. |
| 2016.03.18 | Production release. |

A.2. Compliance and Conformity Statements

A.2.1. CE EMI Conformity Caution

This board is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as the result of modifications to the delivered material is the responsibility of the user.

